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Intermediate Results of a MSI-Based Ripeness and Malformed Classification on an Object- and Pixel-Basis Using FPGA for an Autonomous Strawberry-Harvesting Robot

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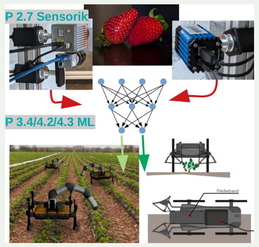
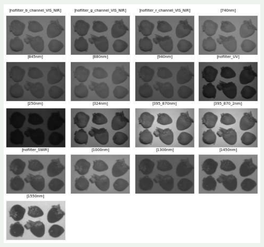
Project RoLand

In RoLand an autonomous in-field strawberry harvesting robot for non-elevated but ground-raised strawberry plants is developed. The robot is supposed to use multi-spectral imaging (MSI) and machine learning (ML) based ripeness classification. Partners in the collaborative research project are the German Research Center for Artificial Intelligence (DFKI), the company Othmerding Maschinenbau, and a strawberry farm.(*)





Approach

Both, an object-oriented and a pixel-oriented approach on RGB-/MSI-camera image data is chosen. At first a Convolutional Neural Network (CNN) is used to classify RGB images into (a) unripe, (b) malformed, or (c) ripe/overripe. As a second step, a pixel-oriented classification on up to 15-dimensional MSI data [2] is supposed to distinguish between ripe and overripe.

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To Summarize

→ Autonomous robot shall classify strawberries as unripe, ripe, overripe, or malformed.

→ Approaches: (1) object-related CNN-based image classification (2) pixel-based 15-dimensional MSI classification

→ To compute CNN classifications on MSI cubes, high computational effort is needed. For an energy-efficient one-chip solution, using FPGAs is one promising option.

Intermediate Results

First tests run on strawberry classification of RGB image data using standard CNN architectures as MobileNet V1 and others. E.g., ImageNet dataset works well as a basis and distinction between unripe and ripe strawberries is reliably possible when adding own training data. RetinaNet was extended to 15-dim MSI data. For pixel-wise classification MLP seems to perform better than SVM. The RGB CNN-classification of malformed strawberries leads to misclassifications. One problem: human pickers have different reasons to select strawberries for disposal, plus: small number of labeled data.

MobileNet V1 was selected as sample architecture to be implemented on an FPGA. Two different approaches: (1) a generic “TPU”-like design and (2) a dedicated design, optimized for this specific application. The latter leads to a power consumption down to 2 W (estimated in simulations) and an inference time of 0.494 ms for a minimized MobileNet V1. Details can be found in [3].

References

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