Hochschule für Angewandte Wissenschaften Hamburg
Hamburg University of Applied Sciences

Bachelor-Thesis

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RC-based oscillator for RF-applications

Fakultät Technik und Informatik
Department Informations- und Elektrotechnik

Faculty of Engineering and Computer Science
Department of Information and Electrical Engineering

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Thema der Bachelor-Thesis

RC basierter Oszillator für Hochfrequenz Anwendungen

Stichworte

RC Oszillator, Relaxation Oszillator, quasi lineares Verhalten, Phasenrauschen

Kurzzusammenfassung

In CMOS Schaltungen ist es üblich, Spulen für LC-Oszillatoren zu benutzen. Diese Spulen nehmen sehr viel Platz im Layout ein. Um die Fläche und die Abstrahlung der integrierten Schaltung zu verringern, kann es sinnvoll sein einen RC-Oszillator zu verwenden. Diese Bachelorthesis beschreibt die Funktion eines Cross-Coupled-RC-Oszillators in 65nm Hochfrequenz CMOS Technologie sowie die Transferfunktion und die Dimensionierung des Oszillators für bestmögliches Phasenrauschen. Es ist eine Kombination von theoretischen Hintergründen, Annahmen und Simulationen, welche am Ende die theoretischen Hintergründe stützen sollen. Abgerundet wird die Arbeit durch eine Zusammenfassung und einen Ausblick auf die nächsten Schritte.

Sebastian Beier

Title of the paper

RC-based oscillator for RF-applications

Keywords

RC oscillator, relaxation oscillator, quasi linear behavior, phase noise

Abstract

In sub-micron CMOS processes LC-oscillators require considerable amount of area because of the integrated inductor. To decrease the die size and to reduce the magnetic field intensity (H-fields) disturbances it can be useful to use a RC-oscillator instead of a LC-oscillator. This work describes the basic function of a Cross-Coupled-RC-Oscillator in 65nm RF CMOS technology. Furthermore, the transfer function as well as the dimensioning for the oscillator for a minimal specified value of phase noise will be given. It is a combination of theoretical views, assumptions and simulations. The simulation results shall confirm the theoretical part as well as the calculation of the component parameters where needed. The summary and a proposal for next steps will complete this work.

Acknowledgement

I would like to thank the company NXP for giving me a place to work and the tools to get my work done.

I would like to thank my supervisors Prof. Dr. Ralf Wendel, Dr. Alexander Mora Sanchez, Dr. Saeed Milady and Ulrich Moehlmann. Saeed Milady and Ulrich Moehlmann especially for giving me hints and very useful advices. Alexander Mora Sanchez for giving me many papers and presentations to learn from and for being my sub investigator.

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1 Introduction

1.1 Thesis organization

This Thesis is organized in 5 chapters. Chapter one is the introduction including the Thesis organisation and the motivation for this Bachelor-Thesis.

Chapter two is the technical background of the relaxation oscillator. It addresses the two different operation behaviors: the non linear and the quasi linear behavior. Developing guidelines for ω_0 and the phase noise and showing the trade-offs one have to consider regarding the achievable frequency of the oscillator, the resistors-size, the capacitor-size, the phase noise and the MOSFETs.

Chapter three is the implementation in Cadence Design Environment, including schematics and simulation parameters.

Chapter four is the simulation and comparison part, where simulation results are shown and a comparison between RC-oscillator and LC-oscillator is done.

In Chapter five the results will be summarized and the simulation results will be compared to the theoretical formulas. Evaluating the outcome and proposing next steps to follow will finish this chapter.

1.2 Motivation

The local oscillator is an integral part of an RF-tuner front-end. It is in charge of generating the so called LO-signal that is fed into the tuners to generate the IF-signal out of the RF-signal. Because of the stringent phase noise specifications, LC-oscillators are used to generate the LO-signal. However, these oscillators tend to be bulky because of the inductor. On the other hand, RC-oscillators are smaller than those based on LC-tanks, at the tradeoff of consuming more power and generating more phase noise.

Nonetheless, there are applications in the RF-area which do not require low phase noise of the LO-signal. In this case, it is desirable to conceive small on-chip LO-generators and, hence, RC-based oscillators could be a feasible option.

The goals of this work are:

- To investigate the operation of an RC-based oscillator, namely, the condition for oscillation, the sizing of the resistor and the capacitor, the attainable frequency as a function of circuit parameters, tradeoff between current consumption and oscillation frequency

- To investigate the attainable phase noise of a function of circuit parameters

- To derive guidelines on the design of a RC-oscillator

- To create at schematic level a RC-oscillator in a 65nm RFCMOS process with the aim of verifying the outcome of the investigate by means of simulations

-To compare the performance of that RC-oscillator with a currently existing LC-DCO

2 Technical background

I decided to take the cross coupled relaxation oscillator for this target because it has very few elements and, in quasi linear behavior, we get a nearly sinusodial high frequency signal with low amount of costs and area.

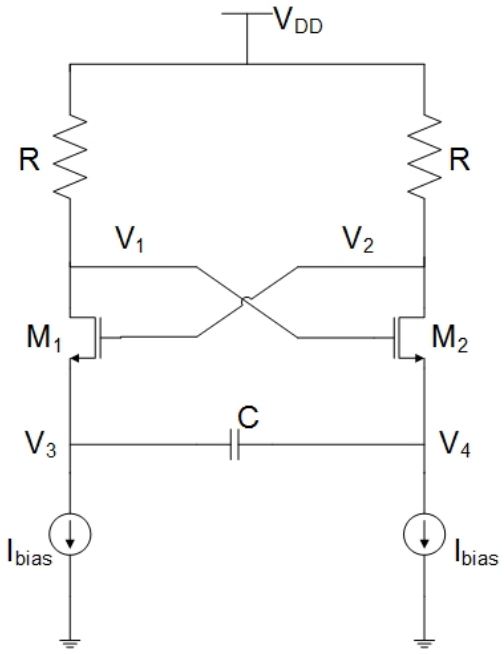

Figure 2.1: Relaxation oscillator

2.1 Principle of operation

To explain the working principle you have to assume an inital state where M_1 is in cut-off region and the capacitor is charged ($V_3 > V_4$), see figure 2.2 - left hand side. No current is flowing through M_1 making V_1 equal to V_{DD}.
The gate voltage of M_2 is higher than the voltage at the source making M_2 conducting. The current of 2I is flowing through M_2 making V_2 equal to V_{DD} - 2RI.
Due to the voltage-difference between V_2 and V_3 the transistor M_1 is not conducting
Now the capacitor is reloaded by the current through M_2. This leads to a voltage decrease in V_3 and a voltage increase in V_4.
The V_{gs} of M_2 decreases and the drain current M_2 decreases as well. Depending on that the drop at R_2 decreases and V_2 increases.
The V_{gs} of M_1 increases and the drain current M_1 increases as well. Depending on that the drop at R_1 increases and V_1 decreases.
The simultaneously decrease of V_3 and the increase of V_2 and vice versa increase of V_4 and the decrease of V_1 is a positive feedback like a Schmitt-Trigger circuit.
A short intermediate state is $V_{gs1} = V_{gs2}$.
V_{gs1} increases and V_{gs2} decreases further so the oscillator will change his state.
Now M_1 is conducting and M_2 is in cut-off region as can be seen in figure 2.2 - right hand side.

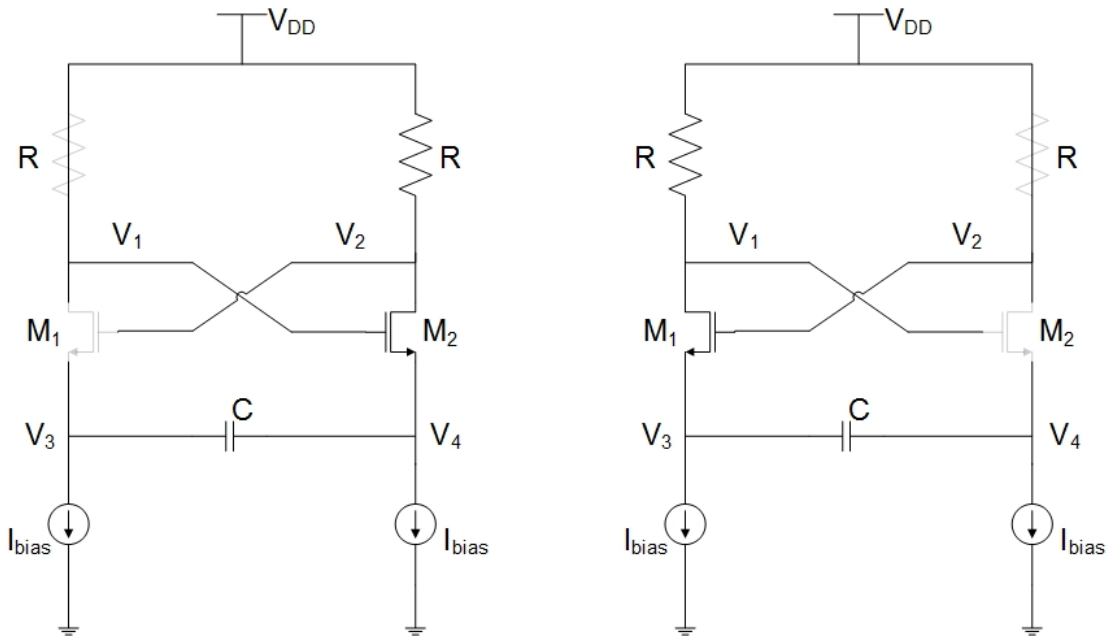

Figure 2.2: Way of working

2.2 Theoretical background

2.2.1 Non linear behavior

The normal workspace of a relaxation oscillator is exremely non linear.

The behavior can be described using the high level model shown in figure 2.3. The output of the integrator, composed of the capacitor and the current sources i_{bias} in figure 2.1, is fed to the input of the Schmitt-Trigger, composed of the resistors and the MOSFETs. The output of the Schmitt-Trigger is fed to the input of the integrator to react to changes of the Schmitt-Trigger. The signals from the high level model are shown in figure 2.4. V_{sch} is a square wave and V_{int} is a triangular wave.

The frequency depends on the time the integrator needs to reach the tresholds. The amplitude is given by the Schmitt-trigger.

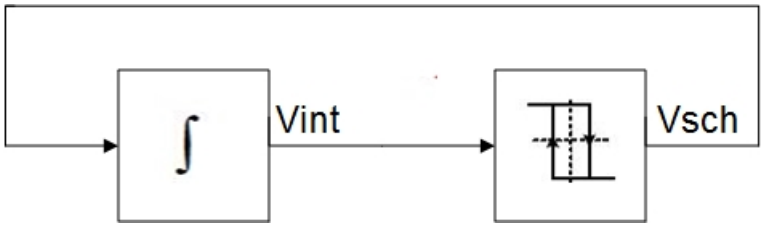

Figure 2.3: High level model

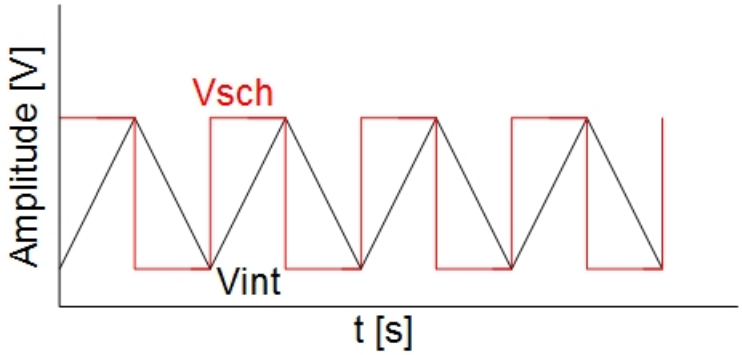

Figure 2.4: Signals from high level model

The differential output of this circuit is equal to V_1 - V_2. Let us assume that the first state is seen in figure 2.2 - (1). With M_1 in cut-off state and current flowing through M_2.

$$V_{out} = V_{DD} - (V_{DD} - 2 \cdot RI) = 2 \cdot RI \tag{2.1}$$

The second state is seen in figure 2.2 - (2). With M_2 in cut-off state and current flowing through M_1.

$$V_{out} = V_{DD} - 2 \cdot RI - V_{DD} = -2 \cdot RI \tag{2.2}$$

This values correnspond to threshold limits caused by the Schmitt-Trigger seen in figure 2.5.

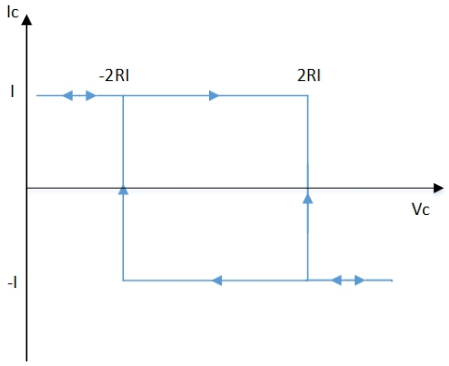

Figure 2.5: Schmitt trigger

The integration constant K_{int} depends on the current flowing through the capacitor devided by the capacitor value.

$$K_{int} = \frac{I}{C} \tag{2.3}$$

The peak to peak voltage is given by

$$V_{PtoP} = 4 \cdot RI \tag{2.4}$$

With equation 2.3 and 2.4 together it is possible to calculate the equation for f_0 in the non linear behavior.

$$f_0 = \frac{I}{2 \cdot C(4 \cdot RI)} = \frac{1}{8 \cdot RC} \tag{2.5}$$

2.2.2 Quasi linear behavior

At higher frequencies transistor parasitics influence the Schmitt-Trigger input impedance putting an additional imaginary part equivalent to an inductor. This gives an equivalent circuit diagram like you can see in figure 2.6. The imaginary part is canceled by the capacitor impedance. This RLC equivalent circuit diagram gives the circuit a quasi linear behavior. The output is nearly a sinewave.

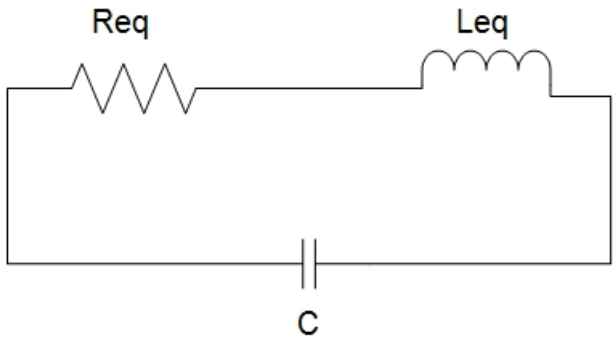

Figure 2.6: Ideal RLC equivalent circuit

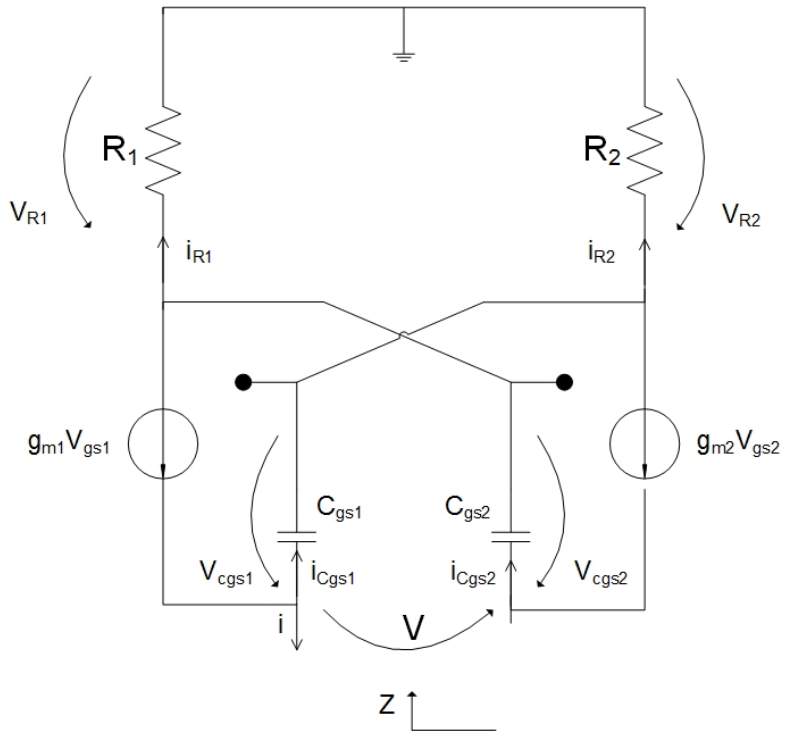

Figure 2.7: Small signal equivalent circuit

$$Z_{in} = 2 \cdot \left(\frac{R \cdot s \cdot C_{gs} - R \cdot g_m + 1}{g_m + s \cdot C_{gs}} \right) \tag{2.6}$$

$$Z_{in} + \frac{1}{sC} = 0 \tag{2.7}$$

$$sC \cdot Z_{in} + 1 = 0 \tag{2.8}$$

$$s^2 + s \left(-\frac{g_m}{C_{gs}} + \frac{1}{2 \cdot RC} + \frac{1}{RC_{gs}} \right) + \frac{g_m}{2 \cdot RCC_{gs}} \tag{2.9}$$

The constant term corresponds to ${\omega_0}^2$

$$\omega_0 = \sqrt{\frac{g_m}{2 \cdot RCC_{gs}}} \tag{2.10}$$

The complete calculation can be found in appendix 6.1

To verify the calculated Z_{in} it is useful to simulate the small signal equivalent circuit diagram.

Using voltage controlled current sources and an AC source as stimuli with 0V DC and 1V AC and compare it to a matlab model that plot the transfer function from Z_{in} in dB over frequency.

The 1V AC has the advantage that the Z_{in} can be directly plotted and only simple calculations are necessary. Simulating the current of the AC simulation and then calculate db20(1/output of the measurement) will lead to the result.

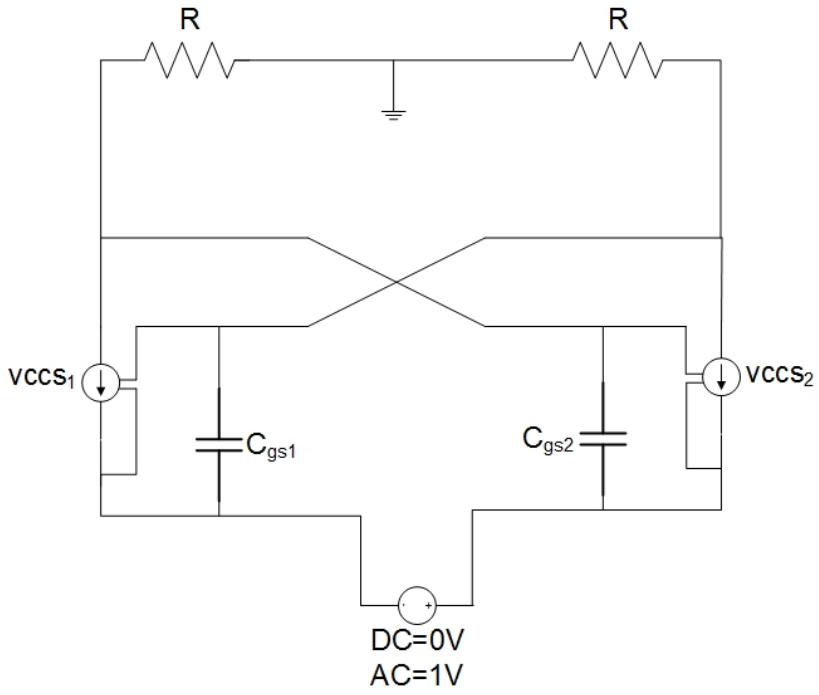

Figure 2.8: Z_{in} schematic proof

The Matlab code belonging to the proof of Z_{in} can be found in the Annex 6.2.

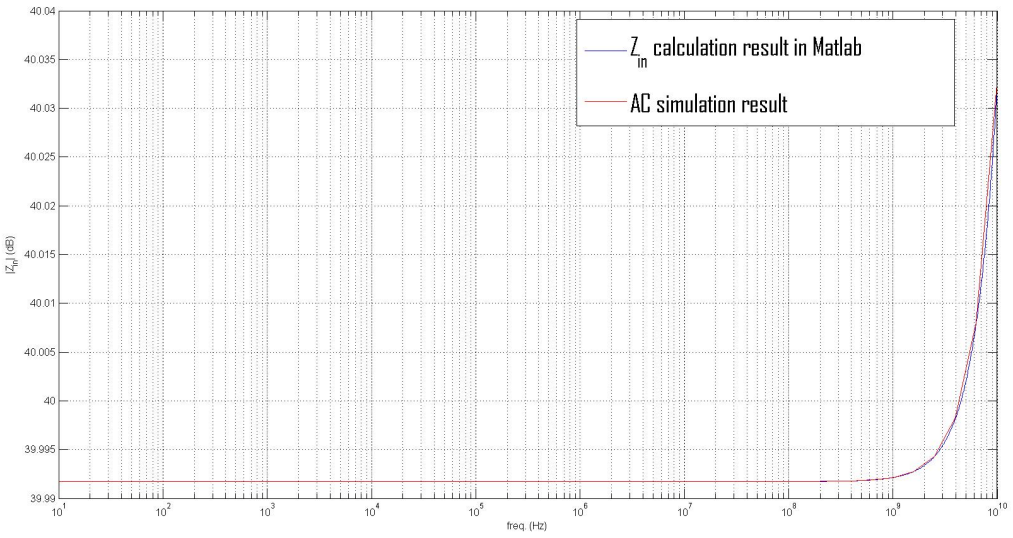

Figure 2.9: Z_{in} simulation proof

The plots are equal so our formula for Z_{in} is correct.

For a more realistical behavior the ideal current sources are replaced by a NMOS current mirror in the design. C_{cm} represents the current mirror transistors. C because only the parasitic effects are mentioned here.

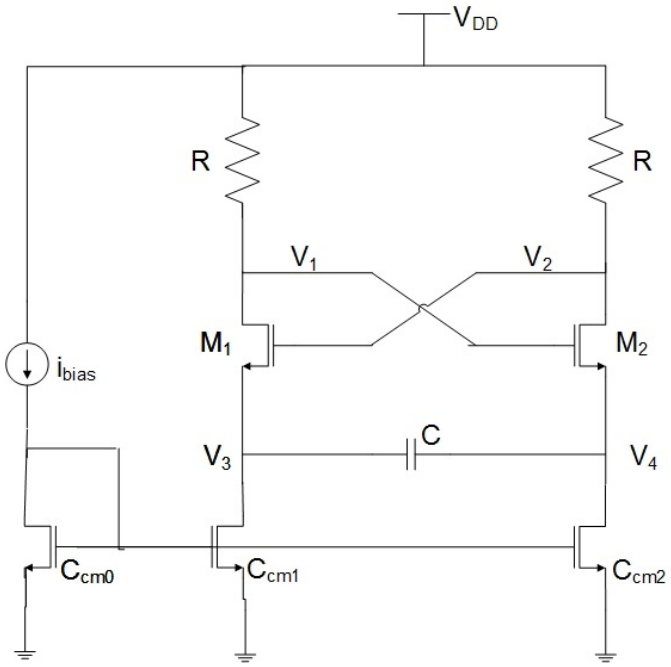

Figure 2.10: Enhanced rc-oscillator circuit

To calculate the new ω_0 one have to redraw the small signal equivalent circuit. To get an better overview both grounds can be connected together, transition from figure 2.11 to 2.12. In figure 2.12 the steady state where M_2 is conducting and M_1 is in cut-off region is assumed.

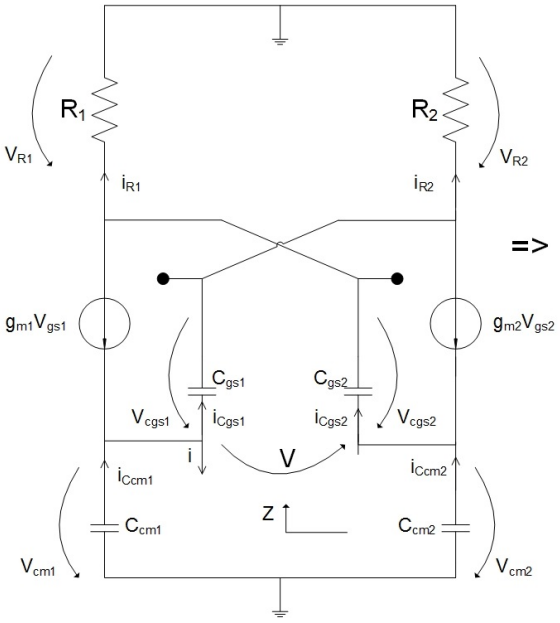

Figure 2.11: Enhanced small signal equivalent circuit

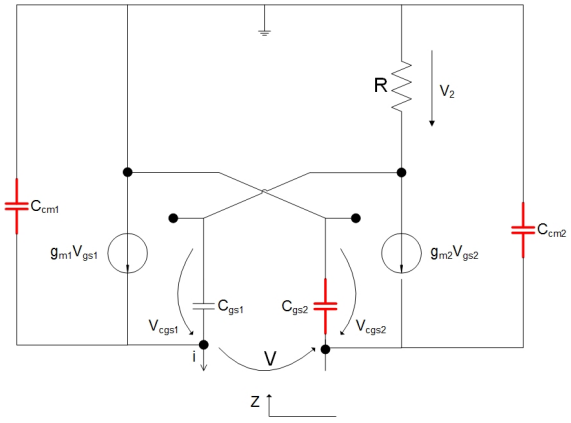

Figure 2.12: Enhanced small signal equivalent circuit adjusted

The new frequency formula is

$$\omega_0 = \sqrt{\frac{g_m}{2 \cdot RC(C_{gs} + 2 \cdot C_{cm})}} \tag{2.11}$$

Now calculating the new variable C_{cm}. Using an AC simulation and a calculation.

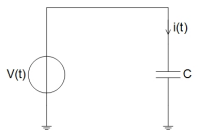

Figure 2.13: Ccm calculation equivalent circuit

$$i(t) = C \cdot \frac{dV(t)}{dt} \tag{2.12}$$

Applying the theoretical formulas to the C_{cm} calculation by simulating the designed circuit in figure 2.10 with the theoretical consideration in figure 2.14 lead to the design in figure 2.15.

$$s = j\omega \tag{2.13}$$

$$\frac{I(s)}{V(s)} = s \cdot C = j\omega C \tag{2.14}$$

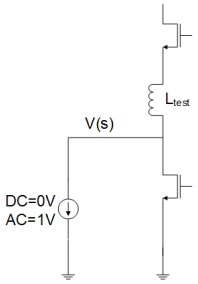

Figure 2.14: Ccm calculation implementation

Using a very high inductor from 1H, named L_{test} to decouple the AC path from the upper circuit part from transistor under test.

$$V(s) = (sC)^{-1} \tag{2.15}$$

$$=> C = \frac{1}{\omega \cdot V(s)} \tag{2.16}$$

Calculation of V(s) on the choosen circuit regarding to the previous coherences of the theoretical background.

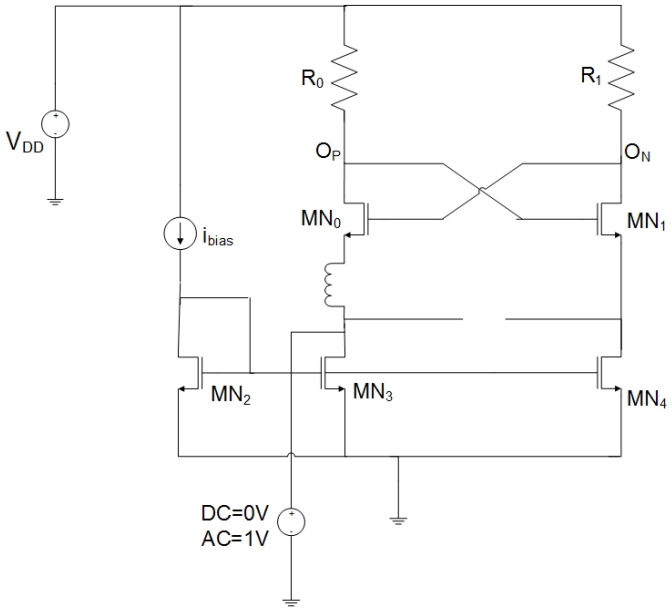

Figure 2.15: Ccm calculation schematic

Output plot of the AC simulation.

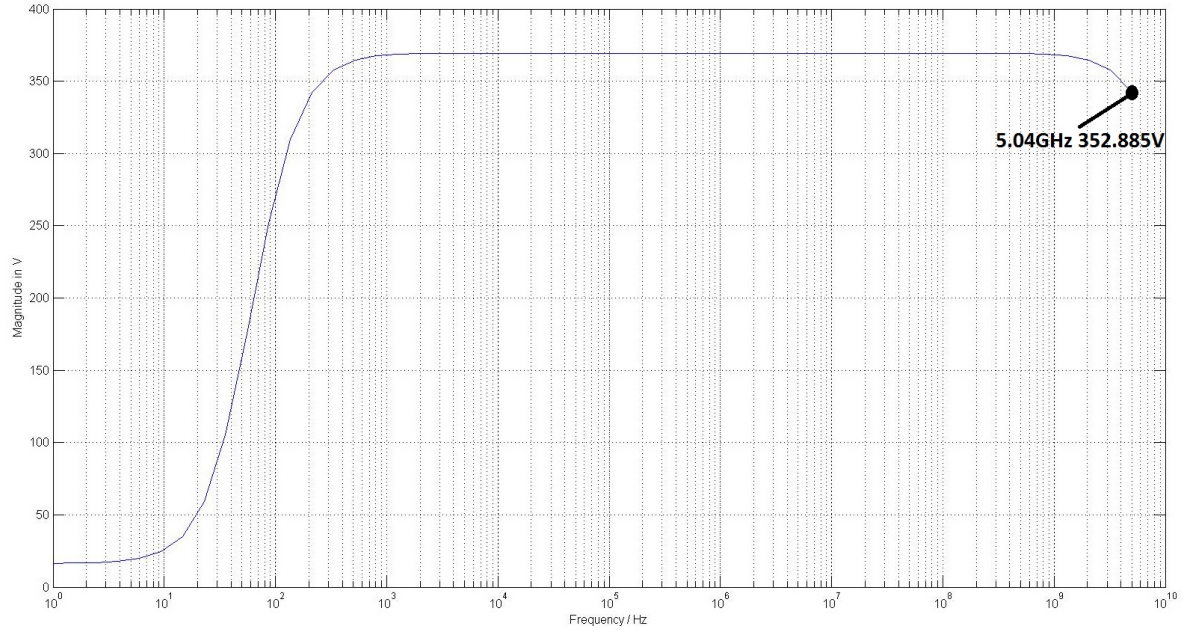

Figure 2.16: Ccm calculation schematic

$$=> C = \frac{1}{\omega \cdot V(s)} \tag{2.17}$$

$$C = \frac{1}{2 \cdot \pi \cdot 5.04GHz \cdot 352.885V} \tag{2.18}$$

$$C = 89,486fF \tag{2.19}$$

The last two missing variables are g_m and C_{gs}. We have to simulate the g_m and C_{gs} of the conducting transistor. Therefor simulating the circuit in steady state, means one transistor is conducting and the other one is in cut-off region, ensured with voltage sources V_{13} and V_{14}, will lead to nearly right values for MN_1. The steady state is an approximation of g_m, since g_m actually varies with time.

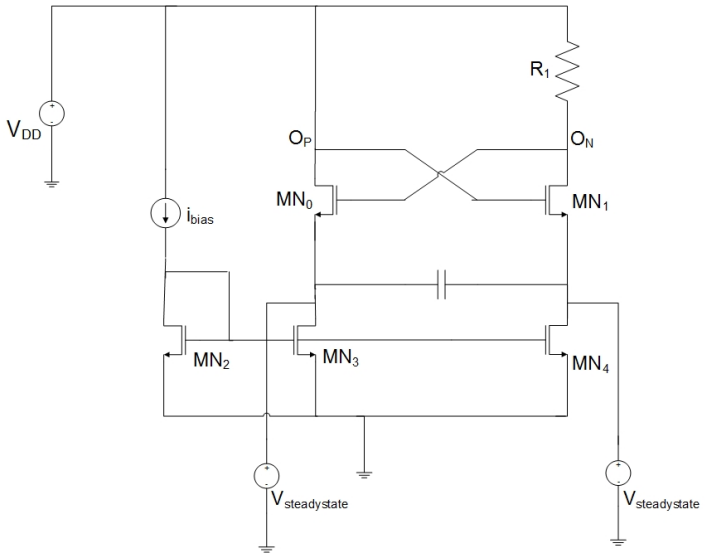

Figure 2.17: Calculating gm and C_{gs} in steady state

MN_1 is the conducting transistor.

g_{m1}	19.98097mS
C_{gs1}	17.83386fF

Table 2.1: Simulation: g_{m0} and C_{gs0}

Now we can calculate the frequency of the circuit.

$$\omega_0 = \sqrt{\frac{gm}{2 \cdot RC(C_{gs} + 2 * C_{cm})}} \tag{2.20}$$

$$\omega_0 = \sqrt{\frac{19.98097m}{2 \cdot 100 \cdot 500f \cdot (17.83386f + 2 \cdot 89.468f)}} \tag{2.21}$$

$$\omega_0 = 3.14218 \cdot 10^{10} \frac{1}{s} \tag{2.22}$$

$$f = \frac{\omega_0}{2 \cdot \pi} \tag{2.23}$$

$$f = 5.07GHz \tag{2.24}$$

2.3 Phase noise

Phase noise is a key element in oscillators as it can significantly affect the performance of RF systems (eg. mixers).

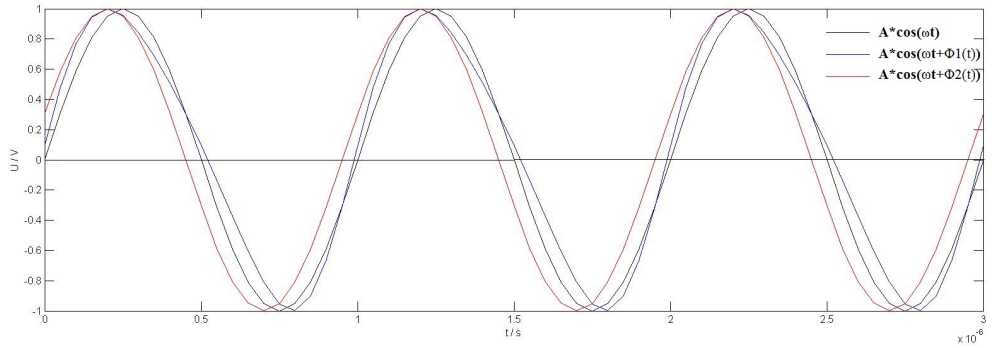

Figure 2.18: Ideal and noisy sinewaves for the topic phase noise

Ideally the oscillator output would be a perfectly periodic sinewave (could be seen in figure 2.18 black line) of the form

$$a(t) = A \cdot cos(\omega t) \tag{2.25}$$

Because of the noisy devices in the oscillator the phase is perturbed at the zero crossings of the sine wave (could be seen in figure 2.18 red and blue line). That leads to the formula:

$$a(t) = A \cdot cos(\omega t + \Phi) \tag{2.26}$$

In the frequency domain the perfectly periodic sinewave would have exactly one peak at the ω_0 frequency (figure 2.19 left hand side). But through the variation in phase we get many more peaks along the phase noise curve with the green curve as envelope (figure 2.19 right hand side).

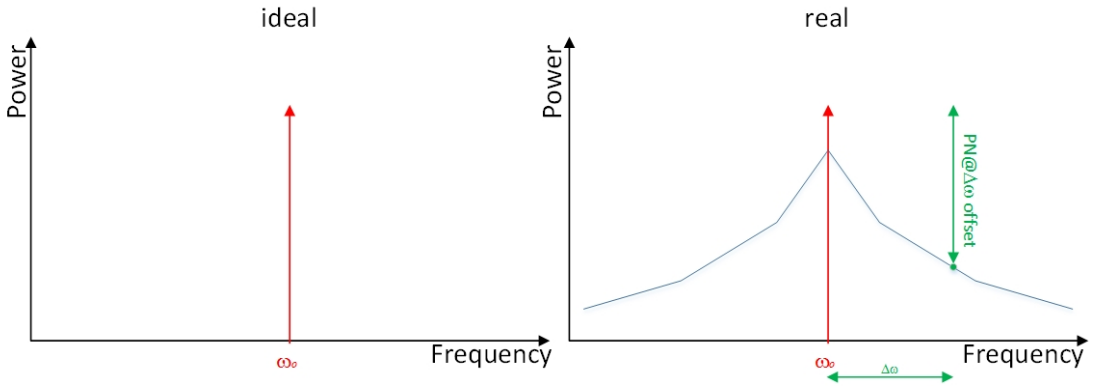

Figure 2.19: Phase noise model

Too high phase noise leads to problems for example when a noisy LO signal with an interferer gets downconverted. When one mixing a carrier signal with a noise free LO signal it gets downconverted without any noise (figure 2.20 left hand side). With a noisy local oscillator and an interferer nearby the carrier signal frequency results in a mixed down noisy interferer, so the carrier signal may disappears in the noise floor (figure2.20 right hand side).

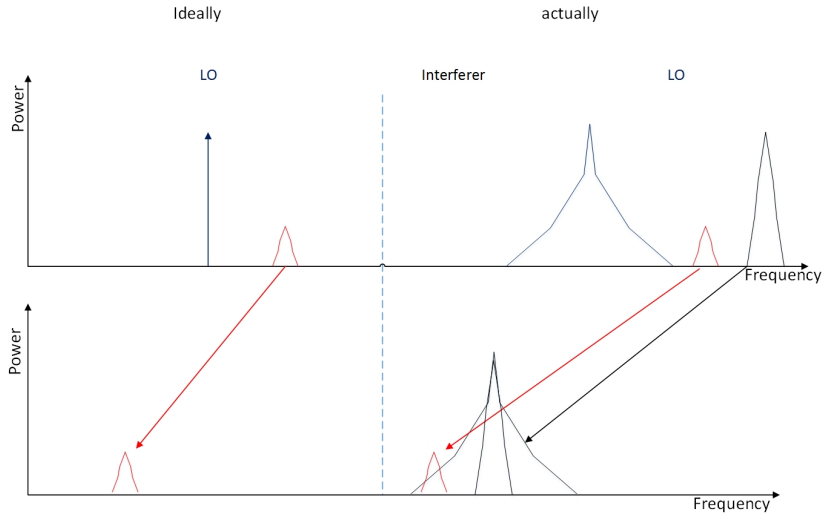

Figure 2.20: Downconverted noisy LO

2.4 Power supply rejection (PSR)

Every circuit needs a power supply. Normally the supply voltage is disturbed by ripple effects.

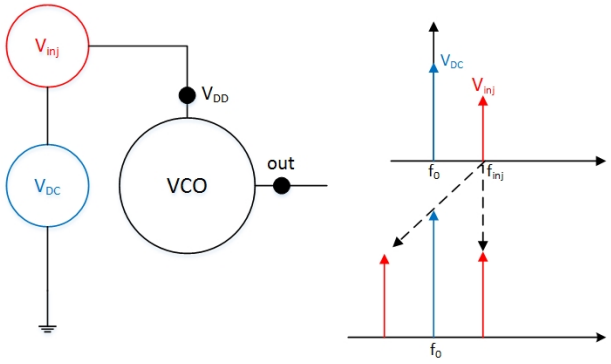

Figure 2.21: PSR mixing

These effects affects the local oscillator resulting in mixing products of the supply ripple frequency and the local oscillating frequency. This results in sidebands around f_0. See figure 2.21. The sidebands can be described with the following formula

$$y(t) = A(1 + \alpha(t)) \cdot cos(\omega + \Phi + \delta(t)) \tag{2.27}$$

that means the amplitude modulation, frequency modulation and phase modulation in the time domain.

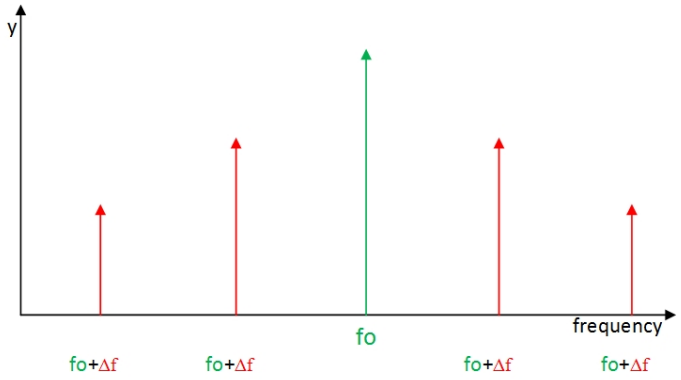

Figure 2.22: PSR sidebands around the oscillator frequency

To calculate this supply voltage ripple effects to the output of the supplied circuit, the power supply rejection analysis is used.

Power supply rejection describes how vulnerable the output of a system reacts to changes of the supply voltage.

To calculate the PSR in dBc a PXF analysis will be performed to determine the conversion gain referenced to the oscillating frequency from the input supply to the differential output of the RC-oscillator.

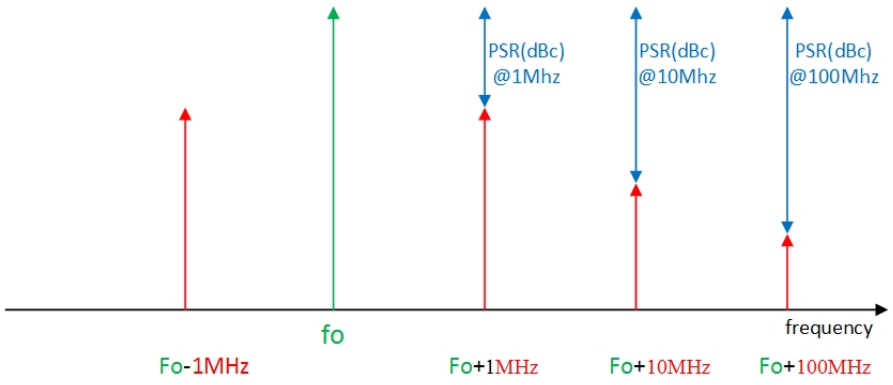

Figure 2.23: PSR calculation in dBc

G_{PXF} is the conversion gain determined by the PXF analysis.

$$PSR(f_0) = G_{PXF}(f_0) \cdot V_{in} \quad (2.28)$$
$$PSR_{dB} = G_{PXF_{dB}} + V_{in_{dB}} \quad (2.29)$$

Example: We assume 5mV as ripple so

$$V_{in_{dB}} = 20 \cdot \log(5m) \quad (2.30)$$
$$PSR_{dB} = G_{PXF_{dB}} + 20 \cdot \log(5m) \quad (2.31)$$

Offset frequency / MHz	PSR / dBc
1	-3.22
10	-23.22
100	-43.22

Table 2.2: PSR calculation for various points

The PSR curve has a drop of -20dB/decade. This is because the circuits behaves like an integrator.

$$f = \frac{d\Phi}{dt} \quad (2.32)$$
$$=> \Phi = \int f\,dt \quad (2.33)$$

2.5 Trade-offs

2.5.1 Metric simulation of phase noise and frequency over resistor value with all other values constant

res	Phase noise / dBc/Hz	frequency / GHz
70	-88.73	7.13
80	-90.16	6.2
90	-90.84	5.53
100	-91.29	5.04
110	-92.25	4.64
120	-93.39	4.31
130	-93.88	4.01

Table 2.3: Parametric simulation results: Phase noise and frequency of oscillator vs. resistor

With a rising value for the resistors the frequency falls and the phase noise gets better. This matches with formular (2.11) for ω_0 because $"R"$ is in the denominator.

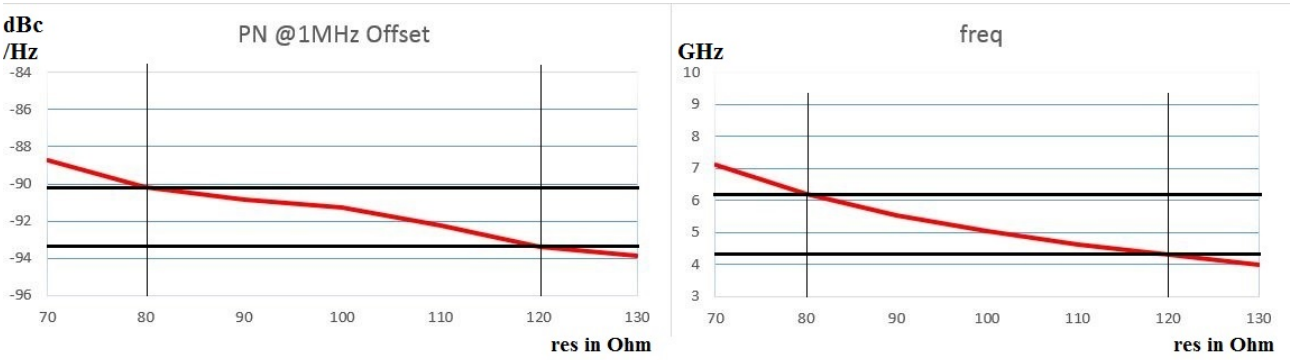

Figure 2.24: Trade-off for phase noise and frequency over resistor R

Assuming a process deviation of the resistors of 20% with a constant independent tail current. Even if the resistor deviation is -20% we can ensure a phase noise better than -90 dBc / Hz and on the other hand at +20% a frequency higher than 4GHz.

Due to the assumed spread of the resistor R it should be taken with a resistance of 100Ω to keep at least -90dBc and a frequency of 4GHz.

2.5.2 Metric simulation of phase noise and frequency over capacitor value with all other values constant

capacitor / fF	phase noise / dBc / Hz	freq / GHz
200	-87.32	9.76
300	-89.19	7.34
400	-90.45	5.95
500	-91.29	5.04
600	-92.38	4.38
700	-92.7	3.89
800	-92.54	3.51

Table 2.4: Parametric simulation results: Phase noise and frequency of oscillator vs. capacitor

With a rising value for the capacitor the frequency falls and the phase noise gets better. This matches with formular (2.11) for ω_0 because "C" is in the denominator.

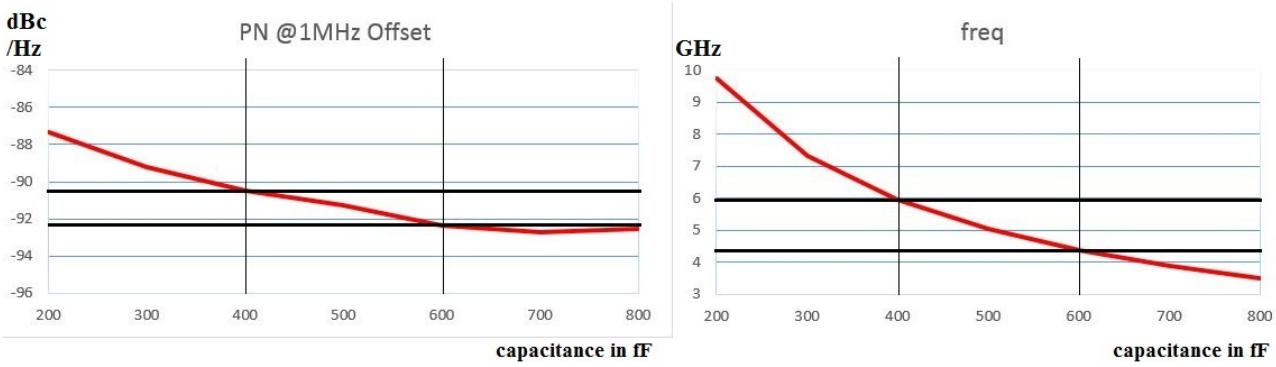

Figure 2.25: Trade-off for phase noise and frequency over capacitor C

Assuming a process deviation of the capacitor of 20%. Even if we have -20% we can ensure a phase noise better than -90 dBc / Hz and on the other hand at +20% a frequency higher than 4GHz.

Due to the assumed spread of the capacitor C it should be taken with a capacitance of 500fF to keep at least -90dBc and a frequency of 4GHz.

2.5.3 Metric simulation of phase noise and frequency over the value of the width of the coupled NMOS with all other values constant

w nmos / μ m	phase noise / dBc / Hz	frequency / GHz
20	-85.69	7.19
30	-89.11	5.91
40	-90.64	5.35
50	-91.29	5.04
60	-92.00	4.83
70	-92.03	4.67
80	-94.47	4.55

Table 2.5: Parametric simulation results: Phase noise and frequency of oscillator vs. width of Nmos

The parametric Analysis of W_{nmos} is a bit tricky. The first thing that comes to mind is, the gm increases - the frequency increases. But the opposite happens. Here we have to look especally to the conducting transistor.

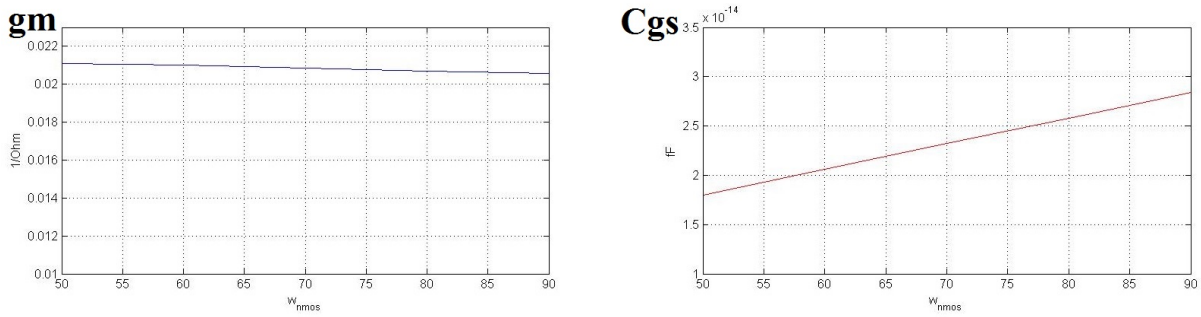

Figure 2.26: Parametric simulation of W_{nmos}

We can see that the gm nearly keeps the same but the C_{gs} rises. Because of that the frequency decreases with a increasing W_{nmos}.

Explanation of constant gm:

$$i_d = g_m \cdot V_{gs} \tag{2.34}$$

$$g_m = \frac{i_d}{V_{gs}} \tag{2.35}$$

i_d and V_{gs} are constant so

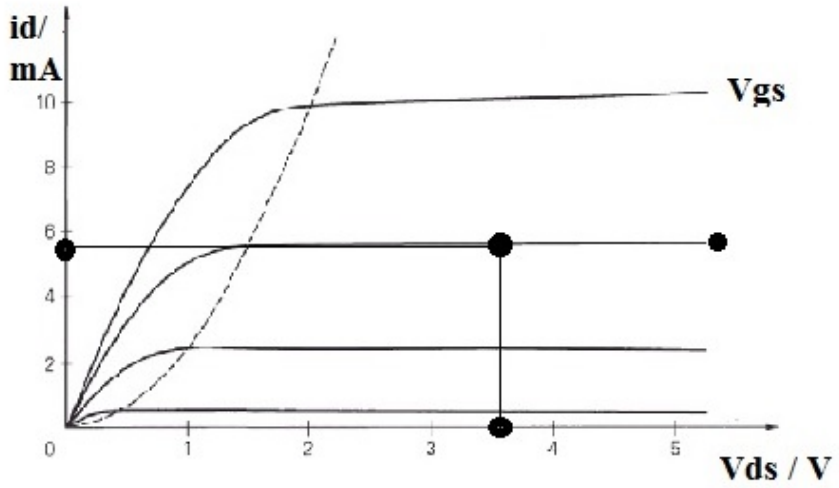

Figure 2.27: Characteristic curve of MOSFET

$$gm = \frac{constantvalue}{constantvalue} \tag{2.36}$$

2.5.4 Metric simulation of phase noise and frequency over the value of the lenght of the coupled NMOS with all other values constant

w nmos / μ m	phase noise / dBc / Hz	frequency / GHz
0.04	-84.52	7.17
0.05	-90.02	5.54
0.06	-91.29	5.04
0.07	-92.34	4.77
0.08	-93.08	4.6
0.09	-93.44	4.48

Table 2.6: Parametric simulation results: Phase noise and frequency of oscillator vs. lenght of Nmos

The parametric Analysis of L_{nmos} is like the one of W_{nmos}. We have to look especally to the conducting transistor.

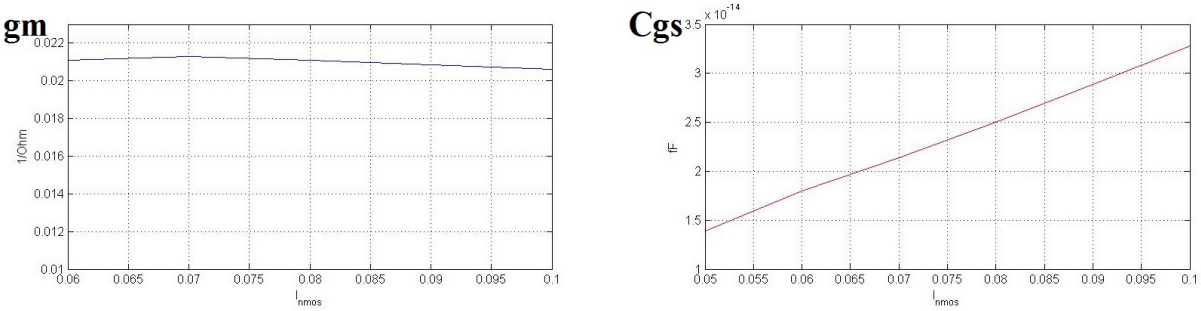

Figure 2.28: Parametric simulation of W_{nmos}

We can see that the gm nearly keeps the same but the C_{gs} rises. Because of that the frequency decreases with a increasing L_{nmos}.

2.5.5 Conclusion

It is not possible to make the frequency and the phase noise better with one variable change. As one can see in the figures 2.29 to 2.32 there is trade-off between the phase noise and the frequency. If one variable gets better the other will get worse. In the diagrams you can see the ratio of frequency divided by phase noise. This leads to a linear slope (blue line). The delta of each step is nearly a horizontal line (orange line). This shows that a change in one parameter leads to a commensurate change in the other direction of the other variable so the ratio is nearly the same every time.

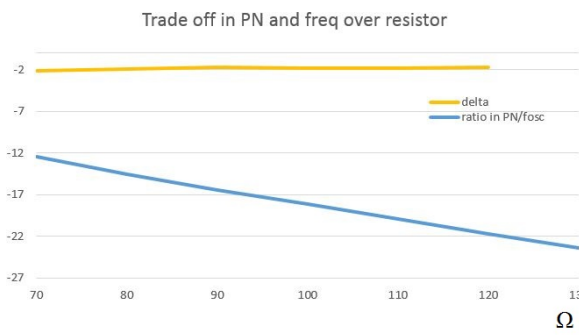

Figure 2.29: Resistor ratio

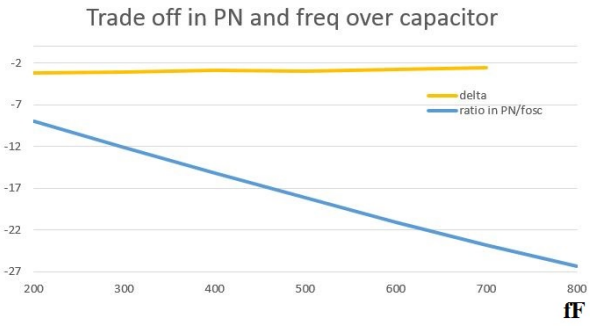

Figure 2.30: Capacitor ratio

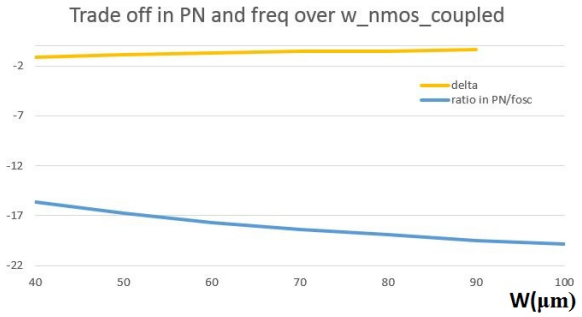

Figure 2.31: Ratio w nmos coupled

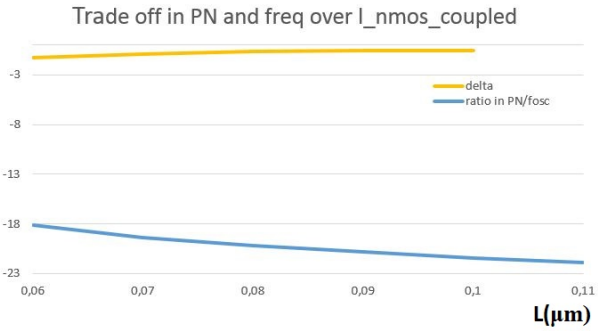

Figure 2.32: Ratio l nmos coupled

3 Implementation in Cadence

In this chapter I will present my designed RC relaxation oscillator operated in quasi linear behavior.

3.1 Schematic

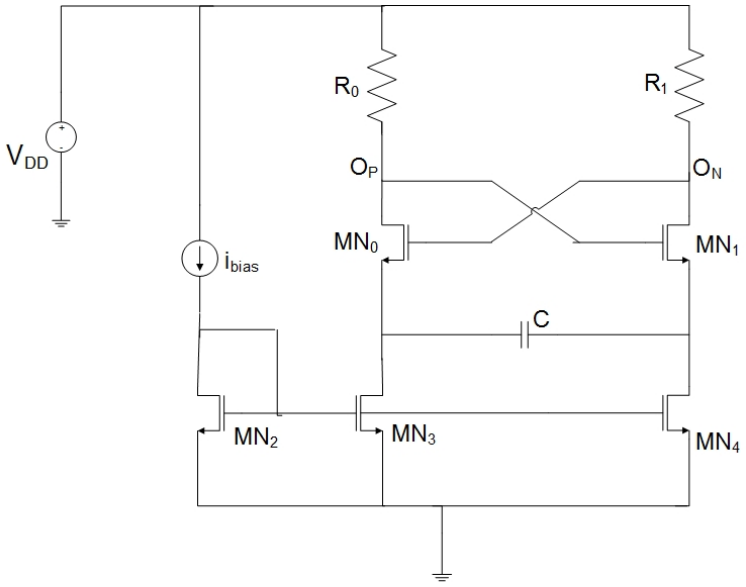

Figure 3.1: Schematic of the designed oscillator

V_{DD}	1.8V
resistor	100Ω
capacitor	500fF
i_{dc}	6mA
W nmos coupled	$50\mu m$
L nmos coupled	$0.06\mu m$
W nmos currmirr	$20\mu m$
L nmos currmirr	$0.06\mu m$
fold	25

Table 3.1: Design of the RC-oscillator

This circuit is a cross coupled RC relaxation oscillator with a current mirror as current sources.

The choosen variables are in my opinion the best compromise between a high frequency and an acceptable phase noise. The variables are choosen to meet the requirements of the 65nm technology and to process variations. See more at 2.4 Trade-offs.

3.2 Other circuits to mention

3.2.1 Cross coupled RC relaxation oscillator with capacitive coupling

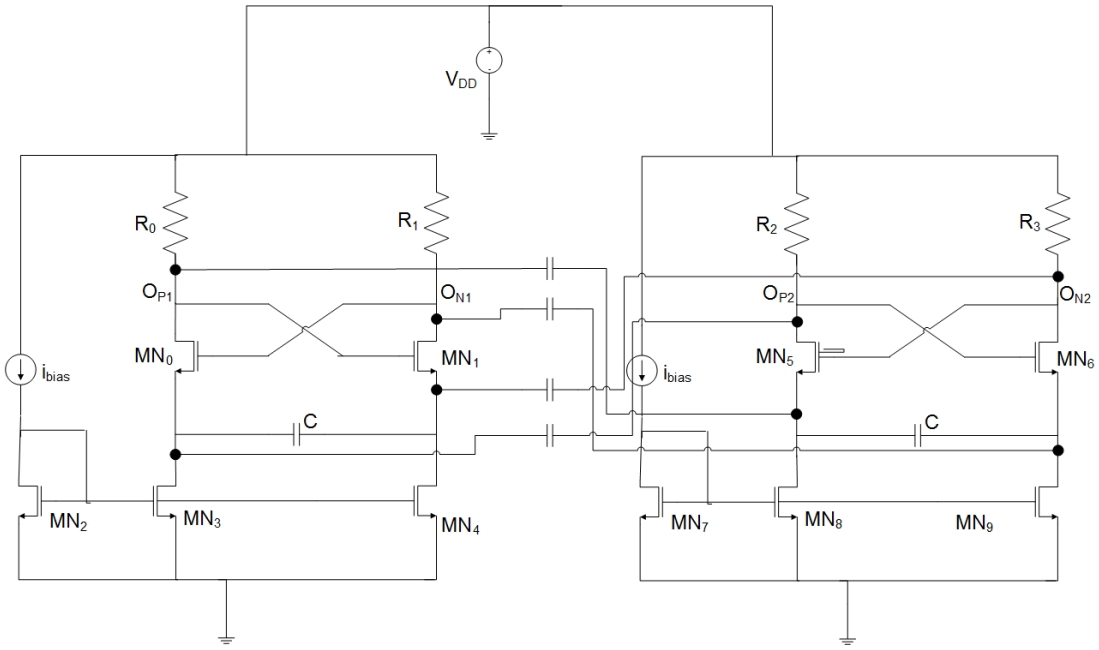

Figure 3.2: Relaxation oscillator with capacitive coupling

The doubled RC relaxation oscillator with capacitive coupling gives a better phase noise with simultaneous higher frequency but at the expense of a higher current and area. In our case this means 6.034Ghz frequency with a phase noise of -101.25dBc/Hz at 1 MHz offset and 33.67mA current. This current and die size is too high for our low cost, low area, low current deployment. But in case that this high current is acceptable the cross coupled relaxation oscillator with capacitive coupling could be a good choice.

3.3 Integrating a buffer

A simulation of the oscillator circuit with a connected real buffer circuit shows the influence of a real load and the buffered output of the overall circuit.

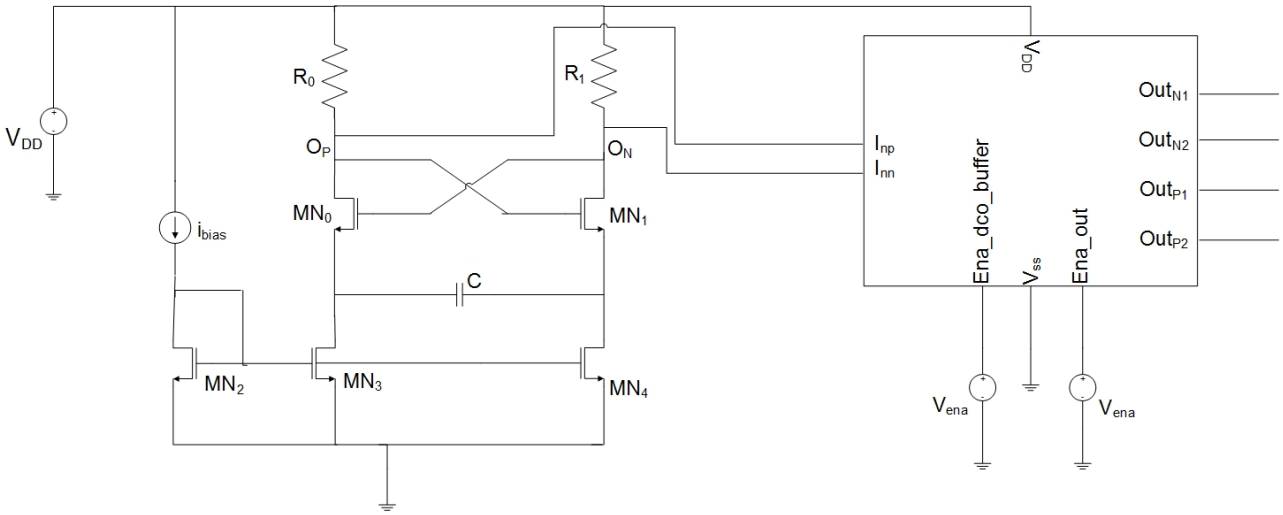

Figure 3.3: Schematic with RC-oscillator and buffer

4 Simulations and comparison

4.1 Designing a RC-oscillator using simulations

The following pages show the simulation results.

Fig. Nr.	description	comment	with buffer
4.1	Frequency over time	Shows that frequency does not vary over time and stays @5.04GHz	x
4.2	Phase noise over frequency offset	Shows the phase noise variation over the frequency offset from the oscillator frequency. Marked is the point @1MHz offset.	x
4.3	Single ended output voltage over time	Shows the single ended output signal of the oscillator. Marked is the peak to peak value.	x
4.4	Gain over relative frequency offset to the center frequency	Shows the continously values related to the discret values in figure 2.22	x
4.5	Frequency over time	Shows that frequency does not varry over time and stays @5.04GHz	✓
4.6	Phase noise over frequency offset	Shows the phase noise variation over the frequency offset from the oscillator frequency. Marked is the point @1MHz offset.	✓
4.7	Single ended output voltage over time	Shows the continously values related to the discret values in figure 2.22	✓

Table 4.1: Overview for simulation resluts with fig. Nr. description and comment

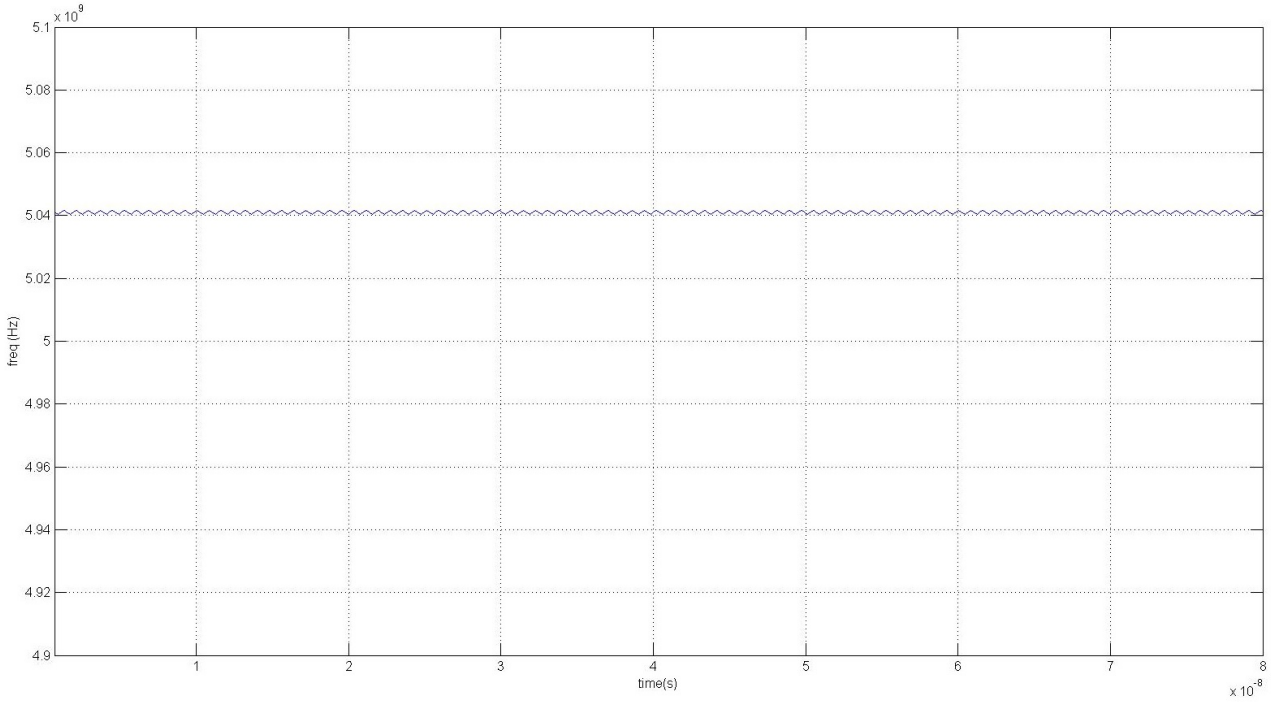

Figure 4.1: Simulation: Frequency over time

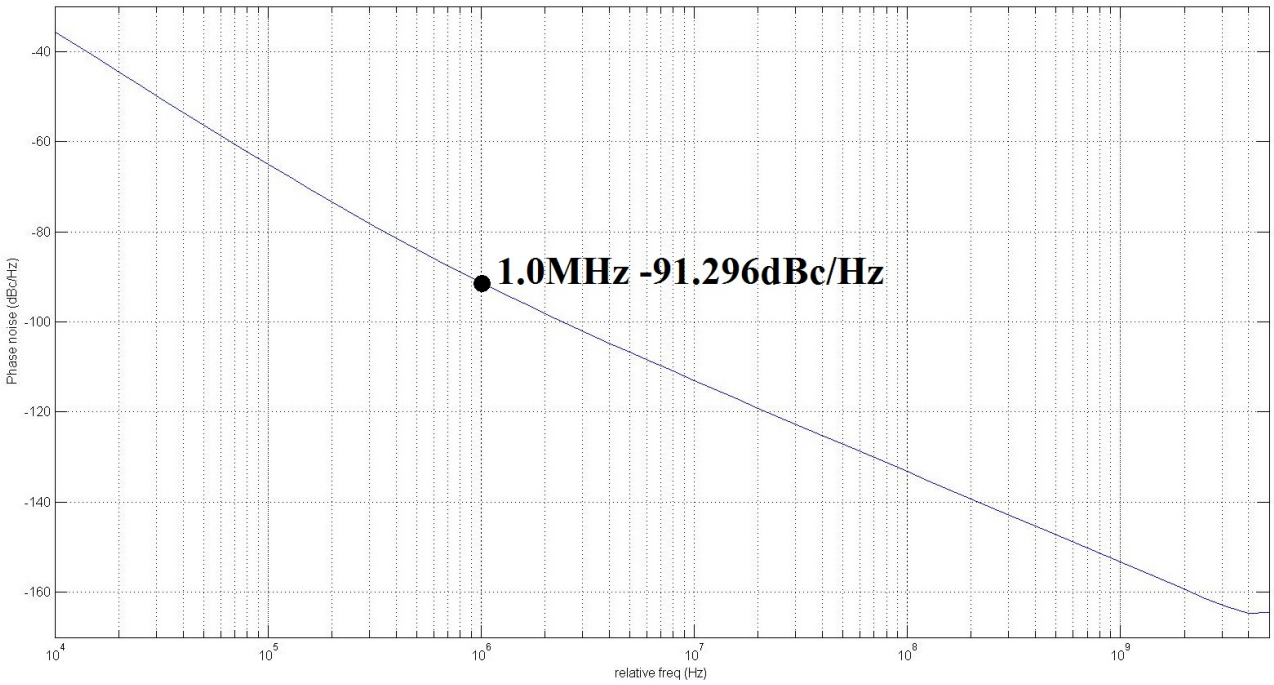

Figure 4.2: Simulation: Phase noise over offset frequency

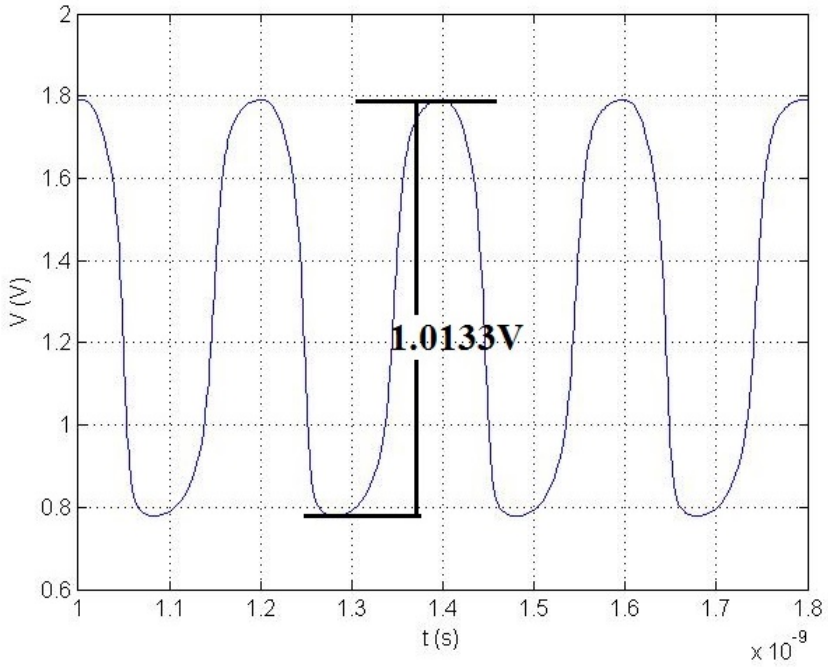

Figure 4.3: Simulation: Output swing over time

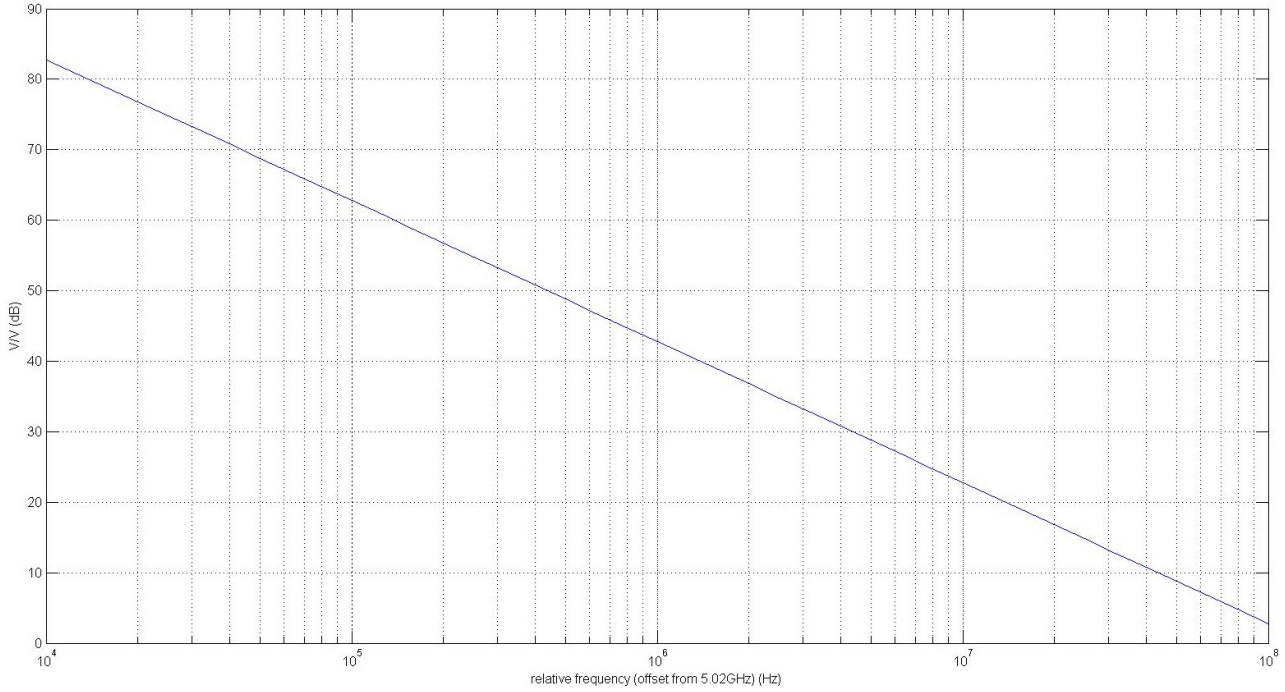

Figure 4.4: Simulation: PSR over relative offset

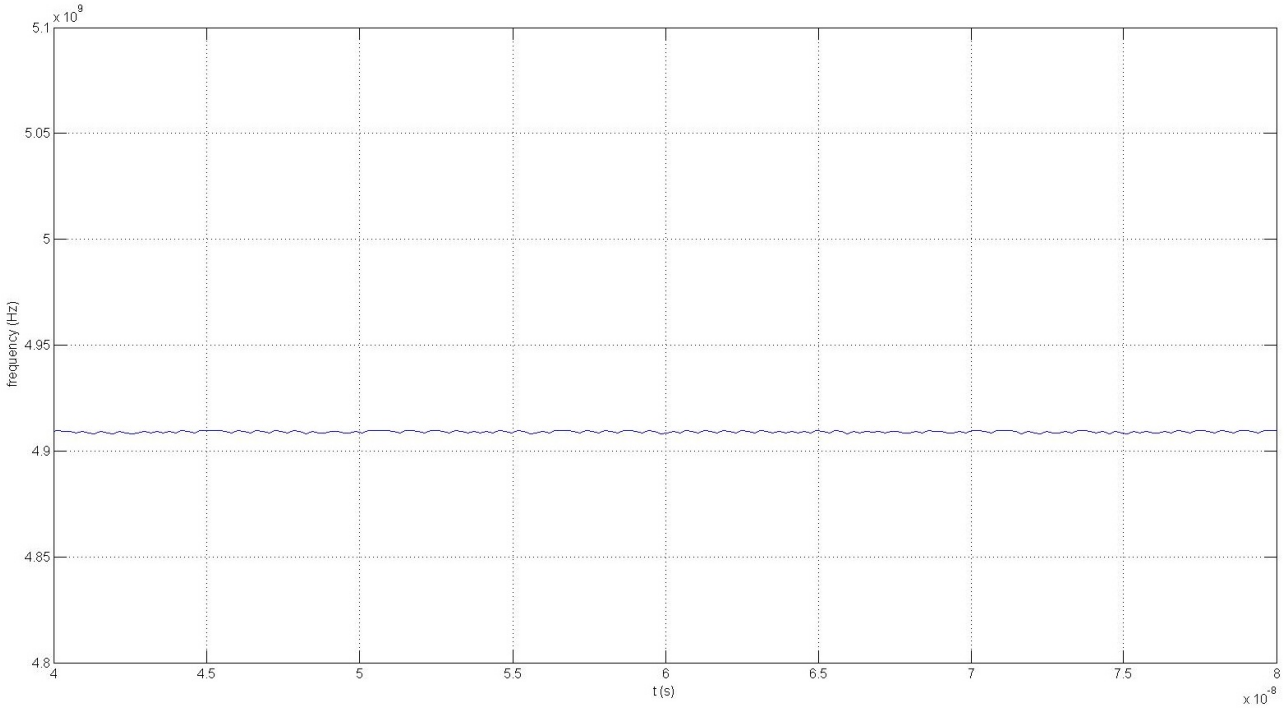

Figure 4.5: Simulation: Frequency over time with buffer

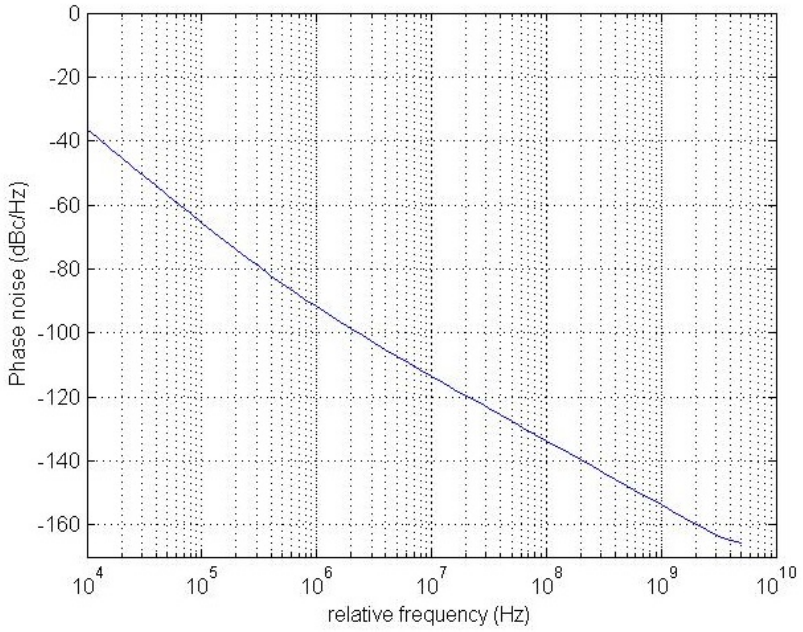

Figure 4.6: Simulation: Phase noise over offset frequency with buffer

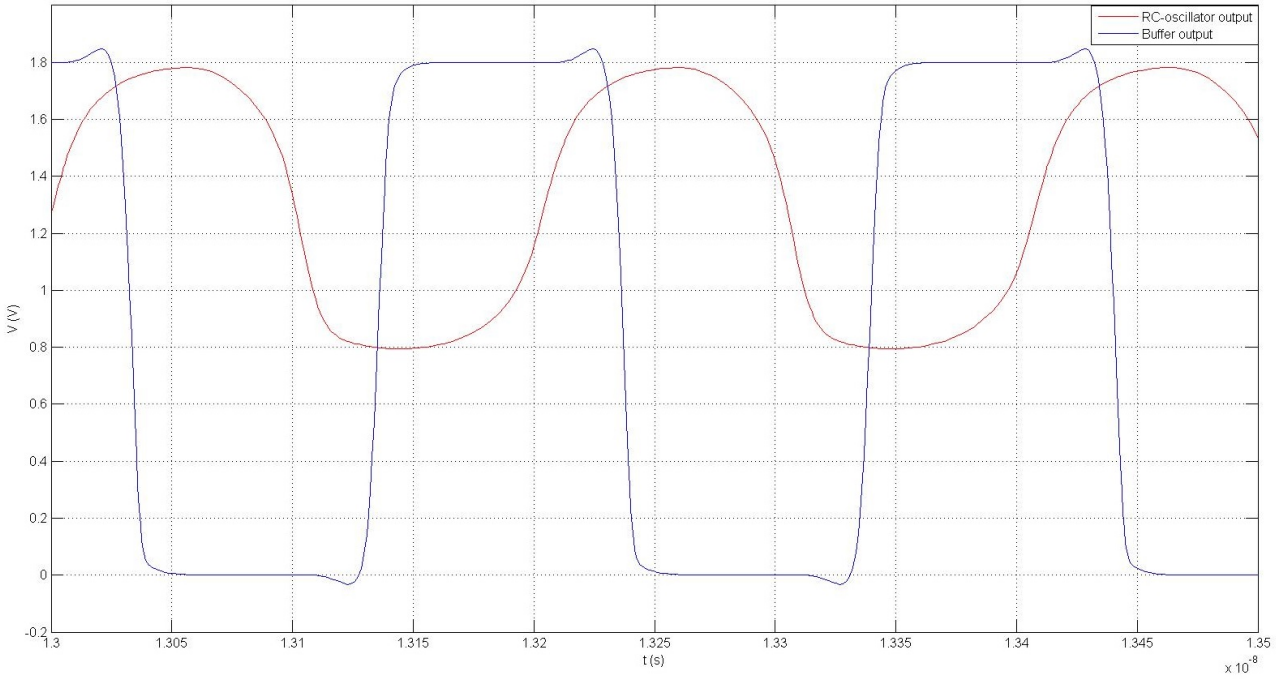

Figure 4.7: Simulation: Output swing over time with buffer

4.2 Current consumption comparison: existing LC- vs. RC-oscillator

Comparing the RC-based oscillator to an existing LC-Oscillator for an ADPLL. We pay respect to the phase noise, the current the circuits need and the output voltage swing. To make them comparable it is necessary to change the resistors to 120Ω - for same frequencies.

In figure 4.8 one can see the schematic of a used LC-Oscillator.

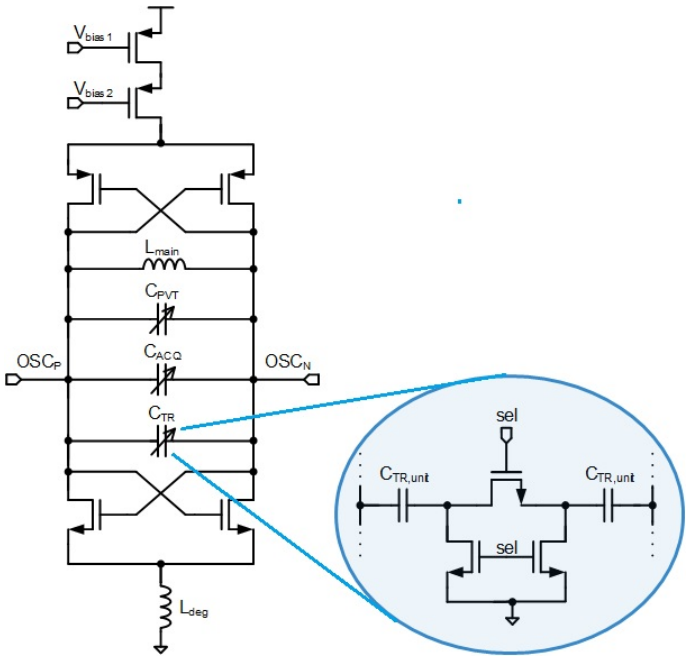

Figure 4.8: LC-Oscillator for comparison reasons

	RC-osc	LC-osc
freq / Hz	4.31	4.31
phase noise / dBc / hz	-93.39	< -110
I / mA	15.9	< 6
output swing / V	1.135	< 1.2

Table 4.2: Comparison LC-oscillator vs. RC-oscillator

It is obvious that the RC-oscillator needs more current for the same frequency and a worser phase noise because of the worser performance. But we can save a lot of area in the die and reduce the H-Field tremendously.

5 Summary and next steps

5.1 Result

I designed a 5.04GHz RC-based oscillator for a PLL circuit with low area used compared to the LC-oscillator. It achieves a phase noise of -91.296dBc / Hz at a frequency offset of 1MHz and a power dissipation of 29.7mW. With the connected buffer the frequency decreases to 4.9GHz caused by the influence of the additional capacitive load. A guideline for RC-relaxation oscillators was created with respect to frequency, phase noise and power supply rejection.

5.2 Comparison of theory and simulation

The theorie matches with the simulated frequency. Calculated 5.07GHz and simulated 5.04GHz. It is a difference of 0.59%.

5.3 Figure of Merit (FoM)

The figure of Merit describes the benevolence of oscillator circuits. It is a good way to compare different circuit types.

$$FoM = L + 10 \cdot log \left[\left(\frac{\Delta f}{f} \right)^2 \cdot \frac{P_{DC}}{P_{ref}} \right] \tag{5.1}$$

L	measured phase noise @1MHz offset	-91.296dBc / Hz
Δf	Offset frequency for phase noise measruing	1MHz
f		5.04GHz
P_{DC}	power dissipation	$1.8V \cdot 16.5mA$
P_{ref}	reference power level	1mA

Table 5.1: FoM

$$FoM = -91.296dBc/Hz + 10 \cdot log \left[\left(\frac{1MHz}{5.04GHz} \right)^2 \cdot \frac{29.7mW}{1mW} \right] \tag{5.2}$$

$$FoM = -113.59dBc/Hz \tag{5.3}$$

5.4 Next steps

-Design a start-up circuit

-simulate the circuit with "real components" for resistor and capacitor

DC, transient, pss, pxf, pnoise, monte carlo

-layout implementation for the design

-extracted layout simulation

-try to decrease the current in relaxation oscillators with capacitive coupling

6 Annex

6.1 Calculation of ${\omega_o}^2$

$$
\begin{aligned}
V_{R1} + V_{cgs2} - V - V_{cgs1} - V_{R2} &= 0 && (6.1)\\
=> v &= V_{R1} - V_{R2} + V_{cgs2} - V_{cgs1} && (6.2)\\
i_{cgs1} &= V_{cgs1} \cdot sC_{gs1} && (6.3)\\
i_{cgs2} &= V_{cgs2} \cdot sC_{gs2} && (6.4)\\
i_{R1} &= i_{cgs2} - V_{gs1} \cdot gm_1 && (6.5)\\
i_{R2} &= i_{cgs1} - V_{gs2} \cdot gm_2 && (6.6)\\
i &= -i_{cgs1} + V_{gs1} \cdot gm_1 && (6.7)\\
i &= i_{cgs2} - V_{gs2} \cdot gm_2 && (6.8)\\
V_{R1} &= i_{R1} \cdot R_1 = (i_{cgs2} - V_{gs1 \cdot gm_1}) \cdot R_1 && (6.9)\\
V_{R2} &= i_{R2} \cdot R_2 = (i_{cgs1} - V_{gs2 \cdot gm_2}) \cdot R_2 && (6.10)\\
R_1 &= R_2 = \frac{1}{G} = R && (6.11)\\
V_{gs1} &= -V_{cgs1} && (6.12)\\
V_{gs2} &= -V_{cgs2} && (6.13)\\
gm_1 \cdot V_{gs1} &= -gm_1 \cdot V_{cgs1} && (6.14)\\
gm_2 \cdot V_{gs2} &= -gm_2 \cdot V_{cgs2} && (6.15)
\end{aligned}
$$

(6.9) and (6.10) to (6.2)

$$v = R \cdot i_{cgs2} - R \cdot V_{gs1} \cdot gm_1 + V_{cgs2} - V_{cgs1} - R \cdot i_{cgs1} + R \cdot V_{gs2} \cdot gm_2 \qquad (6.16)$$

with (6.14) and (6.15)

$$v = R \cdot i_{cgs2} + R \cdot V_{cgs1} \cdot gm_1 + V_{cgs2} - V_{cgs1} - R \cdot i_{cgs1} - R \cdot V_{cgs2} \cdot gm_2 \quad (6.17)$$

from (6.3) and (6.7)

$$i = -V_{cgs1} \cdot sC_{gs1} + V_{gs1} \cdot gm_1 \quad (6.18)$$

with (6.14)

$$\begin{aligned} i &= -V_{cgs1} \cdot sC_{gs1} - V_{cgs1} \cdot gm_1 && (6.19)\\ i &= V_{cgs1} \cdot (-sC_{gs1} - gm_1) && (6.20) \end{aligned}$$

from (6.4) and (6.8)

$$i = V_{cgs2} \cdot sC_{gs2} - V_{gs2} \cdot gm_2 \quad (6.21)$$

with (6.15)

$$\begin{aligned} i &= V_{cgs2} \cdot sC_{gs2} + V_{cgs2} \cdot gm_2 && (6.22)\\ i &= V_{cgs2} \cdot (sC_{gs21} + gm_2) && (6.23) \end{aligned}$$

(6.3) and (6.4) in (6.17)

$$v = V_{cgs2}(R \cdot sC_{gs2} - R \cdot gm_2 + 1) - V_{cgs1}(-R \cdot gm_1 + R \cdot sC_{gs1} + 1) \quad (6.24)$$

From (6.20) and (6.23)

$$V_{cgs1} = \frac{i}{-sC_{gs1} - gm_1} \tag{6.25}$$

$$V_{cgs2} = \frac{i}{sC_{gs2} + gm_2} \tag{6.26}$$

(6.25) and (6.26) in (6.24)

$$v = \frac{i(R \cdot sC_{gs2} - R \cdot gm_2 + 1)}{sC_{gs2} + gm_2} - \frac{i(-R \cdot gm_1 + R \cdot sC_{gs1} + 1)}{-sC_{gs1} - gm_1} \tag{6.27}$$

$$Z_{in} = \frac{v}{i} \tag{6.28}$$

$$Z_{in} = \frac{R \cdot sC_{gs2} - R \cdot gm_2 + 1}{sC_{gs2} + gm_2} - \frac{R \cdot sC_{gs1} - R \cdot gm_1 + 1}{-sC_{gs1} - gm_1} \tag{6.29}$$

with $C_{gs2} = C_{gs1} = C_{gs}$ and $gm_2 = gm_1 = gm$ (6.29) can be rewritten as

$$Z_{in} = 2 \cdot \left(\frac{R \cdot sC_{gs} - R \cdot gm + 1}{sC_{gs} + gm} \right) \tag{6.30}$$

summing Z_{in} with 1 by main capacitance

$$Z_{in} + \frac{1}{sC} = 0 \tag{6.31}$$

$$sC \cdot Z_{in} + 1 = 0 \tag{6.32}$$

$$2 \cdot R \cdot C_{gs} \cdot C \cdot s^2 - 2 \cdot R \cdot C \cdot gm \cdot s + 2 \cdot Cs + gm + sC_{gs} = 0 \tag{6.33}$$

$$s^2 + s\left(-\frac{gm}{C_{gs}} + \frac{1}{2RC} + \frac{1}{RC_{gs}}\right) + \frac{gm}{2RCC_{gs}} = 0 \tag{6.34}$$

constant term correnspond to ${\omega_0}^2$

$$\omega_0 = \sqrt{\frac{gm}{2RCC_{gs}}} \tag{6.35}$$

6.2 Verifying the calculated Z_{in}

z_in.m*

```
gm=19.98097e-3;
R=100;
C=500e-15;
Cgs=17.83386e-15;

s=tf('s');

% z_in formula

Hs = 2*((R*s*Cgs-R*gm+1)/(s*Cgs+gm));

% Define frequency vector from 10^2 to 10^10, 1000 points logarithmically
% spaced

f=logspace(2,10,1000);
w=2*pi*f;

[mag, phase] = bode(Hs, w);

semilogx(f', 20*log10(mag(:)))
xlabel('freq. (Hz)')
ylabel('|z_in| (dB)')
grid
```

Figure 6.1: Z_{in} Matlab Code proof

6.3 CD

An electronical copy of the Bachelor-Thesis can be find on the attached CD.

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Versicherung über die Selbstständigkeit

Hiermit versichere ich, dass ich die vorliegende Arbeit im Sinne der Prüfungsordnung nach §16(5) APSO-TI-BM ohne fremde Hilfe selbstständig verfasst und nur die angegebenen Hilfsmittel benutzt habe. Wörtlich oder dem Sinn nach aus anderen Werken entnommene Stellen habe ich unter Angabe der Quellen kenntlich gemacht.

Hamburg, February 8, 2017	
Ort, Datum	Unterschrift