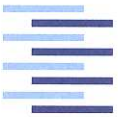

Hochschule für Angewandte Wissenschaften Hamburg
Hamburg University of Applied Sciences

Bachelor Thesis

Andrey Luzhanskij

Development of Measurement Hardware for Electrical and Optical Study of Battery Electrodes

Fakultät Technik und Informatik
Department Informations- und Elektrotechnik

Faculty of Engineering and Computer Science
Department of Information and Electrical Engineering

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Development of Measurement Hardware for Electrical and Optical Study of Battery Electrodes

Bachelor Thesis based on the study regulations
for the Bachelor of Engineering degree programme
Information Engineering
at the Department of Information and Electrical Engineering
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of the Hamburg University of Applied Sciences

Supervising examiner : Prof. Dr.-Ing. Karl-Ragmar Riemschneider
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Title of the Bachelor Thesis

Development of Measurement Hardware for Electrical and Optical Study of Battery Electrodes

Keywords

lithium ion batteries, charging and discharging, optical effects, anode, measurement

Abstract

This thesis is made in assistance to electrical and optical study of lithium-ion-Batteries. This requires ability to precisely set and measure current. A system capable of that is therefore designed and implemented.

Andrey Luzhanskij

Titel der Bachelorarbeit

Entwickling der Messhardware für elektrische und optische Untersuchung der Batterieelektroden

Stichworte

Lithium Ion Baterien, Zellzyklierung, optische Effekte, Anode, Messung

Kurzzusammenfassung

Diese Arbeit dient zur Unterstützung zur elektrischen und optischen Untersuchung der Lithiom-Ion-Batterien. Das erfodert die Möglichkeit, Strom und Spannung genau einzustellen und zu messen. Ein dafür taugliches System wird also entwickelt und relalisiert.

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1. Introduction

1.1. Project BATSEN

The project, which this thesis is based on, emerged inside the BATSEN[1] research group. BATSEN researches innovative methods for monitoring battery condition, especially the State of Health (SoH) and State of Charge (SoC) in different types batteries. For example, in a project, which was funded by the Federal Ministry for Education and Research, a wireless sensor for monitoring of a single battery cell. Likewise, a sensor for optical monitoring of lead acid battery was successfully developed.[1].

Further area of research are Lithium Iron Phosphate ($LiFePO_4$) cells for electric buses. Their longevity and optimal operation are studied on behalf of Hamburg public transportation company HOCHBAHN [49].

The electrodes of the batteries themselves had been optically investigated. It was discovered that optical alterations can be metrologically registered [2].

1.2. Introduction to Lithium Iron Phosphate Batteries

Thereupon comprehensive examination of cell chemistry and the materials for the batteries, comparison of materials for anodes and cathodes, as well as the optical effects on them were performed [2][1] by Jan Grießbach. This section offers short overview of the chemistry of the $LiFePO_4$ cells and optical effects on it based on his work.

A battery is combination of one or several galvanic cells with same internal chemistry in almost all cases. Two fundamental types of batteries are recognized: primary and secondary. The primary batteries have chemistry of galvanic cells with irreversible reactions that makes them non-rechargeable. In contrast, the chemical reaction of the secondary batteries can be reversed by applying external voltage to them, which

[1] abbreviation of “BATtery SENsors”

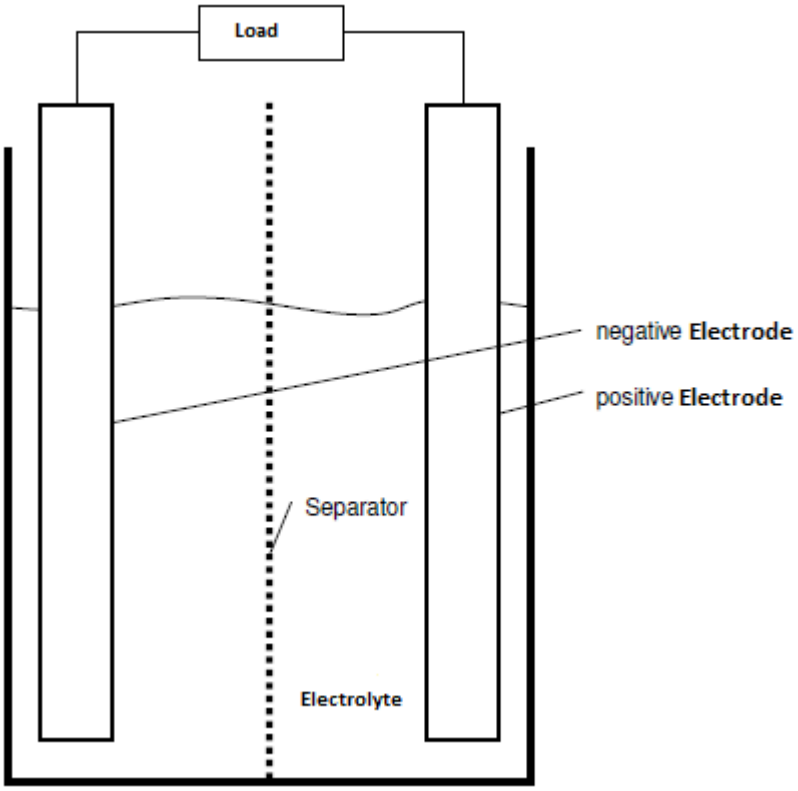

Figure 1.1.: Structure of a galvanic cell. Modified from [1].

causes current through them. The y can by recharged. Secondary batteries are also called *"Accumulators"*. The term "battery" is always referred to the secondary batteries in this thesis.

Figure 1.1 shows the structure of a galvanic cell. It consists of chambers filled with Electrolyte, which are divided by a permeable for ions separator. The positive electrode is located in one chamber, which represents the "plus" pole of the battery. The other chamber contains the negative electrode, which is the "minus" pole of the battery. The Electrodes are also designated with termes "anode" and "cathode". The assignment is dependent on the direction of the chemical reaction.

Anode loses electrons, so it is oxidised.

Cathode accepts electrons, this means it it is reduced.

The negative electrode is the anode and the positive electrode is the cathode during discharging. It is other way round during charging. This thesis uses the terms "anode" and "cathode" from the perspective of discharging.

Lithium ion batteries experience intercalation and deintercalation in addition to oxidation and reduction. Intercalation denote deposition of ions in a host material. The material can change volume during deposition. The deintercalation is the reverse process.

The anode is typically made in of graphite and the cathode of lithium metal oxide or lithium metal phosphate.

1.2.1. Optical Effects on the Electrodes

A research group has discovered measurable optical changes on the graphite anode during charging process of the battery . The intercalation of Li+ ions in the graphite turns the gray black electrode into red-brown during the charging process. BATSEN has confirmed this scenario by an independent observation using test battery models [54].

This effect takes place as a result of lithium ion intercalation into graphite electrode. Therefore, it is believed that this change in the graphite layered structure could be useful in fiber optical sensor measurements for battery life estimation [54].

Similar observation that performed in anode has practised on the positive electrode (cathode). During the tests $LiFePO_4$ was used as the metal oxide for the cathode. The results proved again a strong optical change on the cathode. The lithiation process that takes place in lithium ion phosphate electrode results in a chemical change from $Fe(III)PO_4$ to $LiFe(II)PO_4$. This shift of concentration from Fe(III) to Fe(II) causes changes in ion bonds and crystal structure which leads to an optical absorption behaviour [54].

The task of this thesis is development of hardware in assistance to research of the optical effects on the *cathode*.

The observations have to be performed by a microscope camera that has a built in illumination with LEDs [1]. However their intensity is fixed. To enable research under different lighting intensity and spectrum conditions team member S. Pereguda developed an alternative system. It consists if six 3-channel LEDs (red, green, blue), whose intensity can be individually controlled .

1.3. Cycling of the Batteries

In order to investigate the above described optical effects and their correspondence to electrical processes/behaviour/state as well as other properties of the battery,

the cell needs to be cycled. Cycling means controlled charging and discharging of a battery. Typically the battery is charged up to or discharges down to a certain voltage. Then a break is made for a certain *convalescence time* to allow the battery to settle [55]. After that the process is reversed and repeated.

The main modes of charging and discharging are:

Constant current (CC) : the battery is subjected to constant charging or discharging currents [55].

Constant voltage (CV) : a contant voltage is applied to the battery.

Constant current constant voltage (CC/CV) is a combination of the other two. The battery is charged or discharged in the CC mode. When it is close to its target voltage the charging or discharging is switched to constant CV mode.

2. Description of the Project

2.1. Description of the Previous System for Battery Cycling

The first design and assembly of a measurement station with a Camera, Spektrometer as well as modular n control and analysis software foe optical observation of SoC of lithium cells was developed by Jan Grießbach [1][2]. The system lacked internal voltage and current measurement, and was unable to charge and discharge in CC mode.

The next version and immediate predecessor of this work was developed by T. Geist [3] for his bachelor thesis. His system consists of measurement printed circuit board with different integrated circuits and analogue devices and the Raspberry Pi 2 single-board computer running Raspbian[1] operation system. It controls the hardware on the board and receives the measurement data over SPI-bus and GPIO pins and saves it on external storage. Simultaneously, the images of the anode are taken every 10 seconds with the microscope camera and evaluated. Additional components on board are dedicated to controlling luminosity of the LEDs and measuring of the temperature.

The cycling of the battery includes charging and discharging in CC mode, which requires maintaining a constant current through the battery. Figure 2.1 illustrates the general idea for the regulation of the current by T. Geist, which happens in a dynamic control loop. Software on Raspberry Pi sets the current regulator on the measurement board. It reads the voltage and current values from onboard voltmeter and ammeter and incrementally adjusts the current to the set value until a preset voltage limit of the battery cell is reached. The controlling software was originally developed by T. Geist. It was then extensively overhauled by N. Rieckmann[2]. The previously mentioned hardware components are described below in more detail.

[1] A derivative of Debian Linux

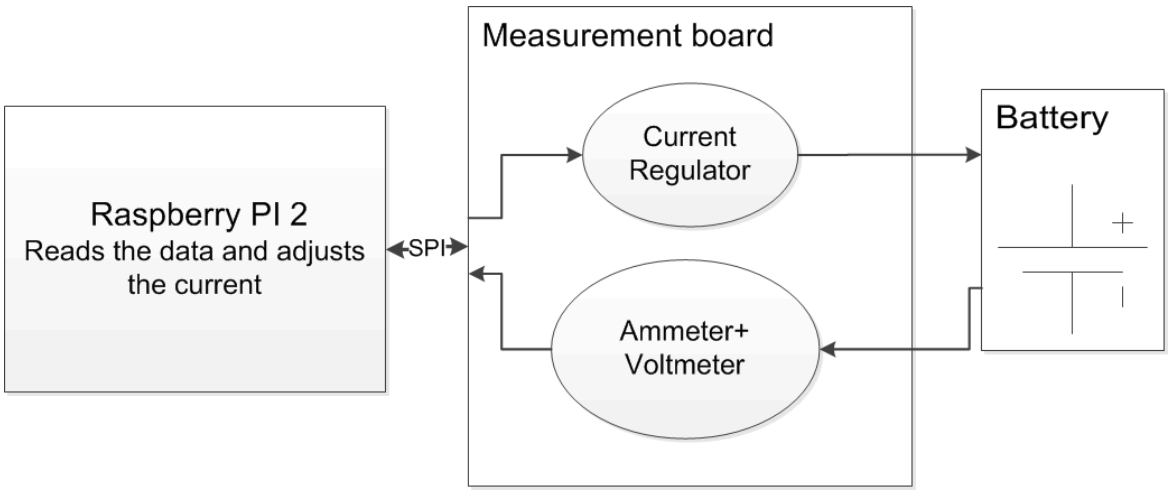

Figure 2.1.: Principle function of the current regulation

2.1.1. Current Regulator

The basic operation of the current regulator module in the previous syten, is shown on Figure 2.2. The charging/discharging current is produced by introducing a difference between the output voltage of the OPA743 operational amplifier and the voltage on the cathode of the battery on the terminals of the shunt resistor R_s.The current can be varied by changing the output voltage with AD5680 DAC thus changing the voltage across R_s. The convention accepted in this thesis as well in the preceding works is the current to the battery (charging, amplifier sourcing) corresponds to positive current, and the current from the battery (discharging, amplifier sinking) corresponds to negative current. Assuming R_s being equal to 100Ω (as on the previous expansion board) the charging/discharging current is:

$$I = \frac{U_{out} - U_{cath}}{100} \tag{2.1}$$

Charging or discharging the battery causes the change of the battery voltage, and thus of the voltage difference across R_s and therefore of the current. That is why the software controller has to compensate continually by adjusting the DAC voltage.

The AD5680 DAC has nominal resolution of 18 bit. However, the 2 LSBs are achieved by interpolation, which were unused. The reference voltage of U_{ref}=2.5V together amplifier gain of G=2 results in 5V as effective maximum output voltage of the current regulator. The LSB is then equals $LSB = 5\,\mathrm{V}/2^{16} \approx 76.3\mu V$, which results in the smallest step for current regulation of $76.3\mu V/100 = 0.763\mu A$.

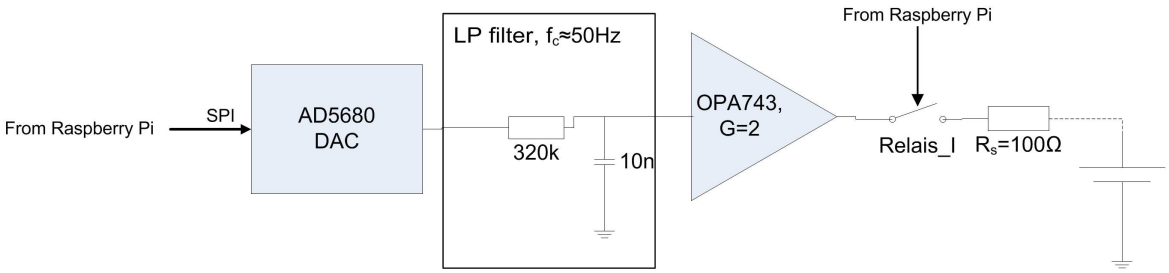

Figure 2.2.: Simplified presentation of composition of the current regulator module

A low pass filter is supposed to reduce the noise of the DAC output. Its cut off frequency:

$$f_c = \frac{1}{2\pi \cdot 320\,\mathrm{k} \cdot 10\,\mathrm{nF}} \approx 50\,\mathrm{Hz} \tag{2.2}$$

In addition, the relay *Relais_I* turns the current flow on and off.

2.1.2. Ammeter

The composition of the ammeter is depicted in Figure 2.3. The AD8422 instrumental amplifier is used because of high-impedance inputs and to get the difference of the voltages on the terminals of the shunt resistor R_s (the same as in Section 2.1.1). The output of the instrumentation amplifier is connected to AD7691 ADC, which is supposed to digitise it. However, since the analogue inputs of the ADC are unipolar, the output of the instrumentation amplifier is shifted by 1.25V by the means of the reference input. Additionally, the amplifier gain G is set to 10 to better utilise the 2.5V range of ADC set by external reference. Considering the ADC has 18 bit resolution, of which 17 bits are effectively used (see Section 2.2 for explanation), the conversion of the digital output D of the ADC to current value is performed according following formula:

$$I_{measured} = \frac{D \cdot \frac{2.5\,\mathrm{V}}{2^{17}} - 1.25\,\mathrm{V}}{G \cdot R_s} = \frac{D \cdot \frac{2.5\,\mathrm{V}}{2^{17}} - 1.25\,\mathrm{V}}{1000} \tag{2.3}$$

2.1.3. Voltmeter

The composition of the voltmeter is depicted on Figure 2.4. The AD8422 instrumentation amplifier serves as high input impedance buffer for battery voltage. Its output

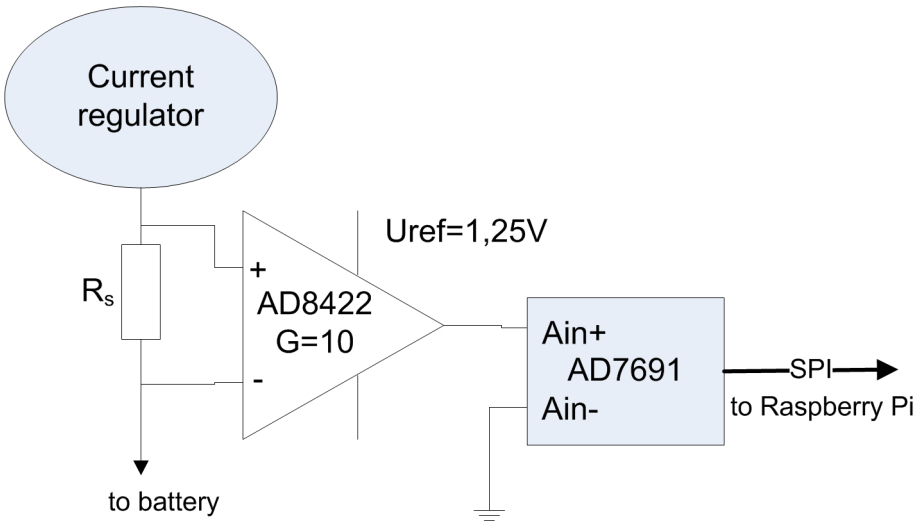

Figure 2.3.: Block diagram the Ammeter module

is digitised by AD7691 18 bit, ADC of which 17 bits are effectively used (see Section 2.2 for explanation). Its full scale is set to 2.5V by external voltage. However, since the battery voltage can be significantly higher, that is why the output of the instrumentation amplifier is halved by an 1:2 voltage divider. The formula for calculating the measured voltage from the digital output D of th ADC is then:

$$U_{measured} = D \cdot \frac{2.5\,\mathrm{V}}{2^{17}} \cdot 2 \tag{2.4}$$

The relay's Relais_VP and Relais_VN connect the battery to the charging/discharging electric circuit.

2.1.4. LED control

The LEDs are controlled with the help of pre-existing external driver developed by S. Pereguda. This circuit accepts analogue voltages from 0 to 5 V, and has the reverse effect on the luminosity: at 5 V the driver dims the LED, while at 5V the LED has maximum luminosity. This voltage is controlled by the 10 bit AD5271 digital potentiometer.

2.1.5. Temperature Measurement

The temperature measurement is performed by external 16 bit LM74 sensor. The board provides 3.3 power supply as well as SPI bus connector.

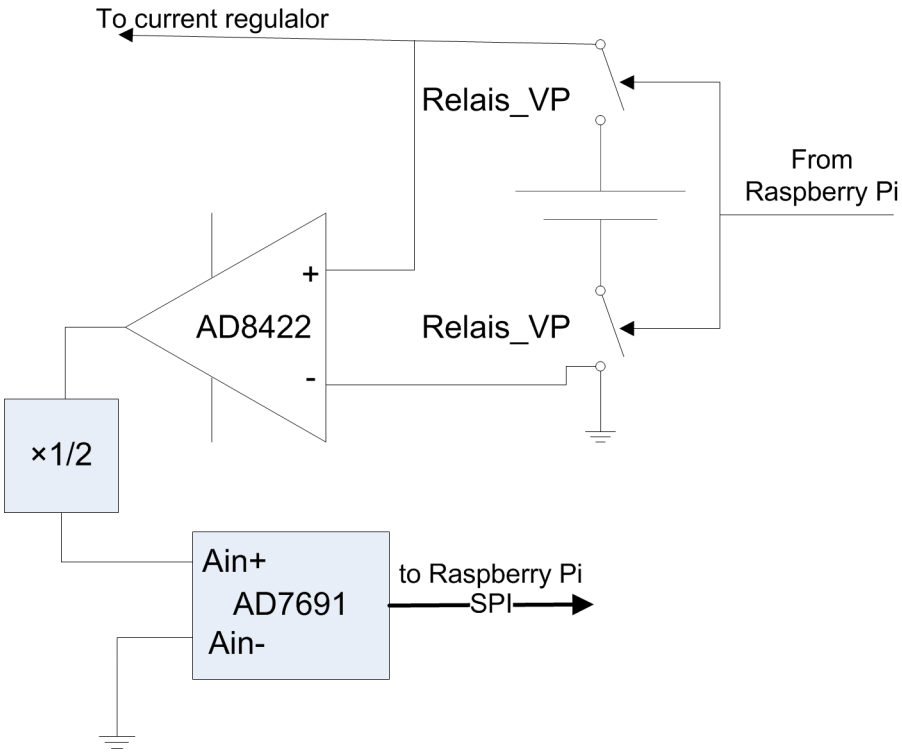

Figure 2.4.: Block diagram of the voltmeter module

2.1.6. Power Supply

An external power supply unit provides a negative and a positive voltage. Internally, the board has multiple voltage levels. Here is a list of voltage levels together with their application:

- 10V (LM2940T-10.0). Used by:
  - Postive power supply of OPA743 operational amplifier and 2×AD8422 instrumentation amplifier as well as 5V levels
- 2×5V (MAX8881) for digital and analogue power supply:
  - Analogue: Power supply for AD5680 DAC and 2×AD7691 as well as 2.5 and 1.25 voltage levels
  - Digital: Coils of the relay's, load voltage of the AD5271 potentiometer and 3.3 voltage level
- 3.3V (TLV2217):
  - Power supply for digital interfaces and sets level for logical "high" of SPI bus.
- 2.5V (TPS79925):
  - it is supposed to provide reference voltage for 2×AD7691 ADCs and the AD5680 DAC
- 1.25V (LD39015):
  - reference voltage for AD8422 instrumentation amplifier in the ammeter circuit
- -10V(LM7910CT)
  - Negative power supply of 2×AD8422 instrumentation amplifiers

Analog and digital grounds are separated and connected only at one point.

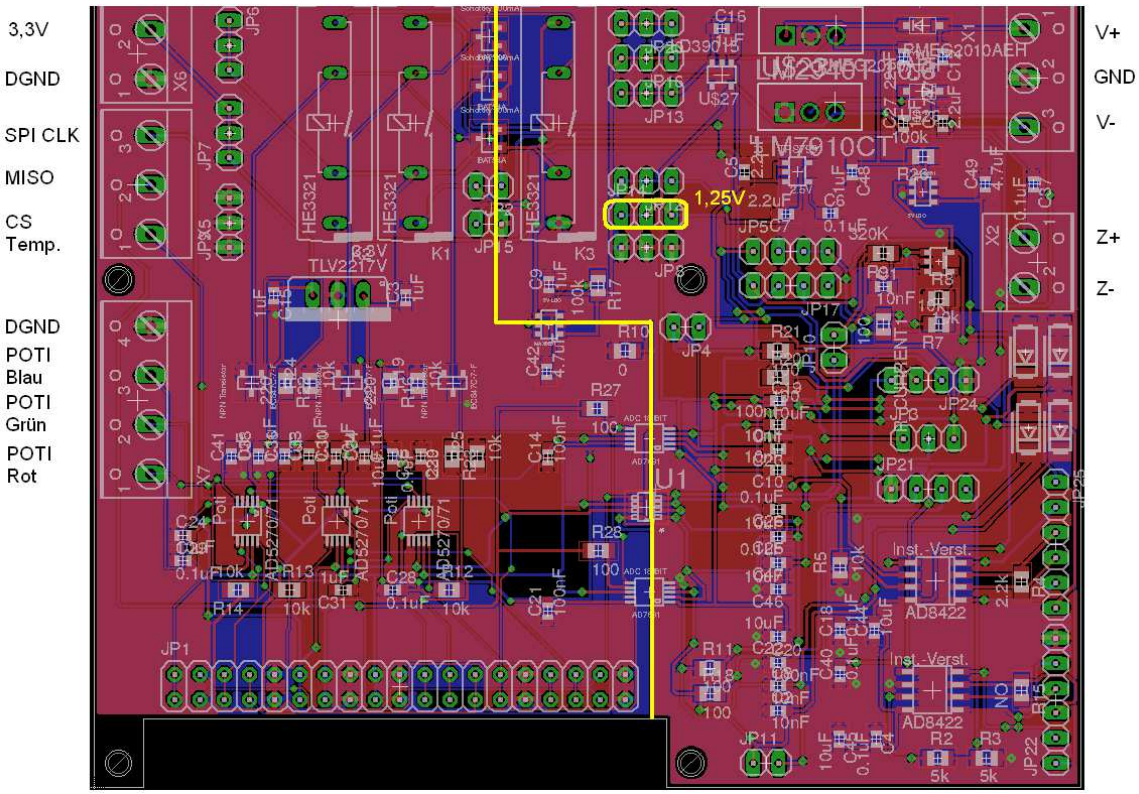

Figure 2.5.: Eagle layout of the PCB with external clamps designated. Taken from [3]

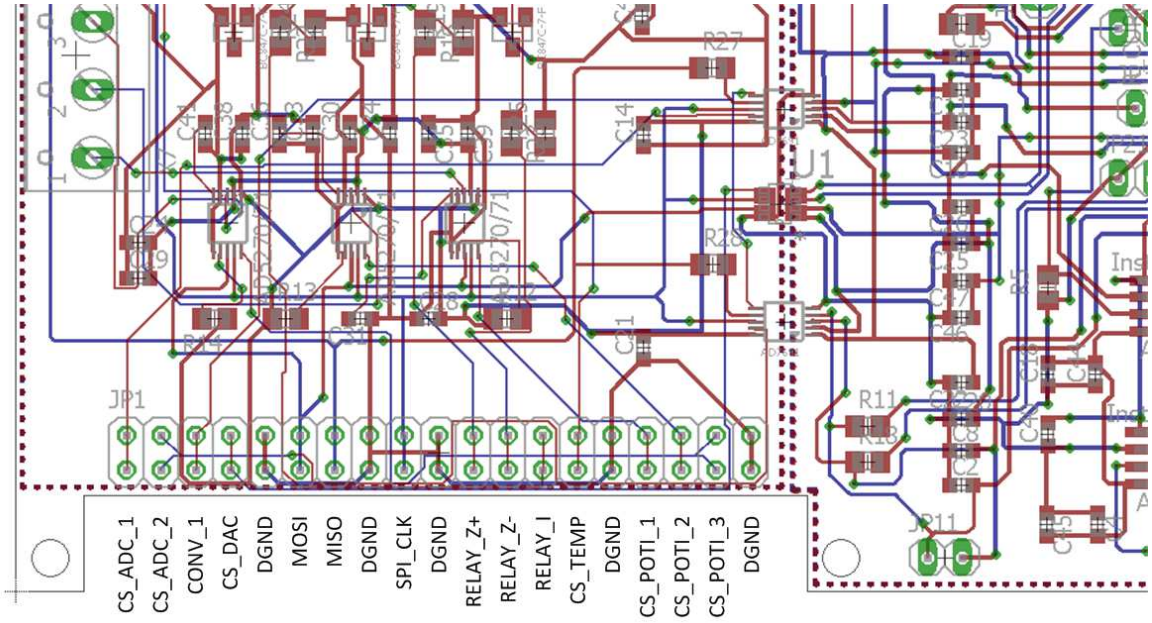

Figure 2.6.: Pinout of the measurement board

2.1.7. Hardware Implementation

The layout (Figure 2.5) of measurement PCB was developed in Eagle CAD software [3]. He made an effort to separate analogue and digital circuitry both electrically and spatially in attempt to prevent mutual interference. The board communicates with Raspberry Pi over cables connected through 19×2 pinhead. The rows are duplicate. The pinout is shown on the Figure 2.6.

The board assembled with SMD technology is presented on Figure 2.7.

2.2. Description of Problems and Errors

Unfortunately, the board did not function as expected after putting it into operation. Already tests early (Figure 2.8) showed inaccuracy of 3 μA and noise up to 5 $\mu A_{p\text{-}p}$, despite attempted software filtering and averaging. Later test runs pointed to even larger noise [2].

The analysis of the previous design revealed numerous shortcomings:

1. Some components chosen are not suitable:

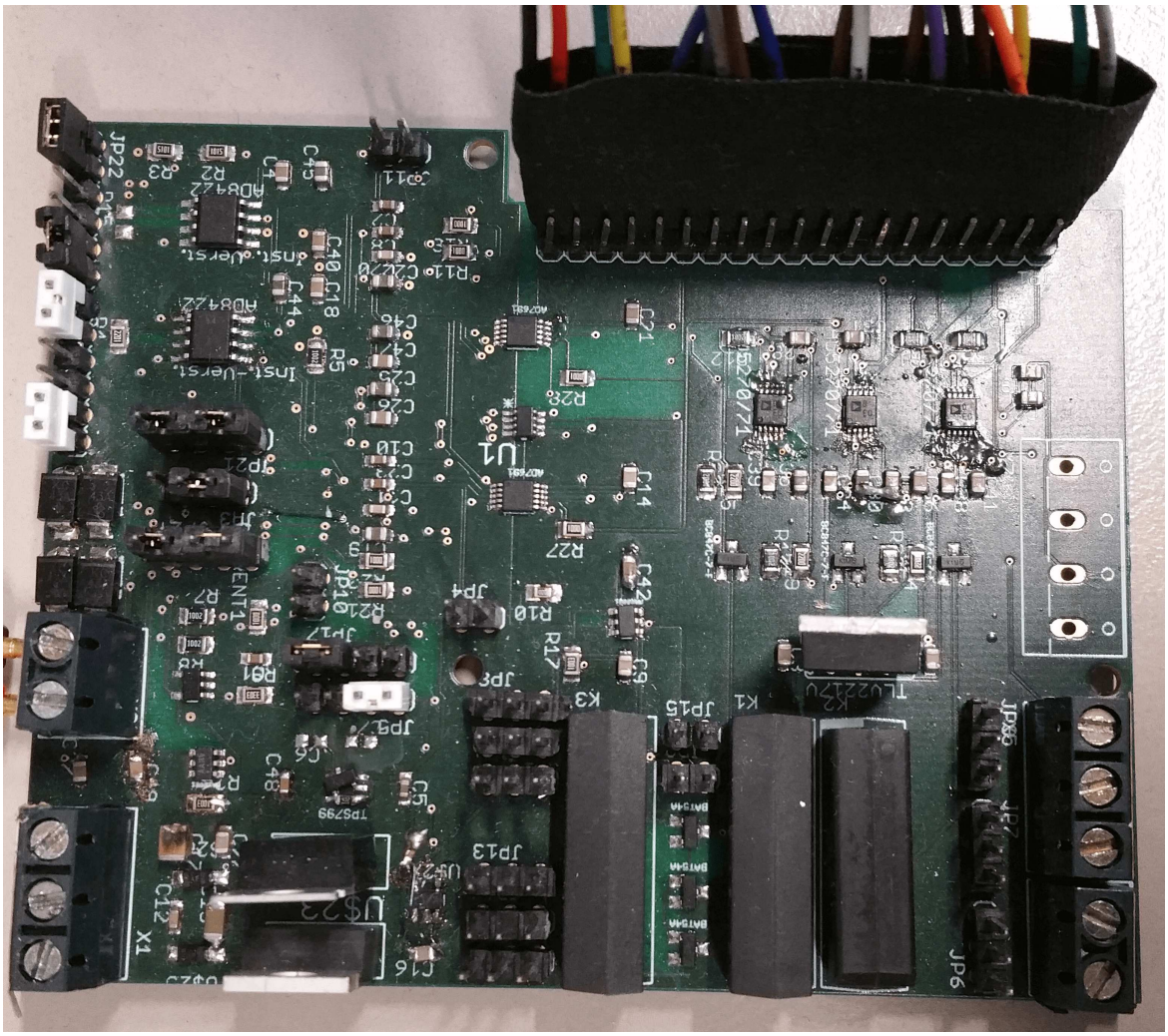

Figure 2.7.: A view on the assembled measurement board with changes described in section 2.2.1. Taken from N. Rieckmann [2]

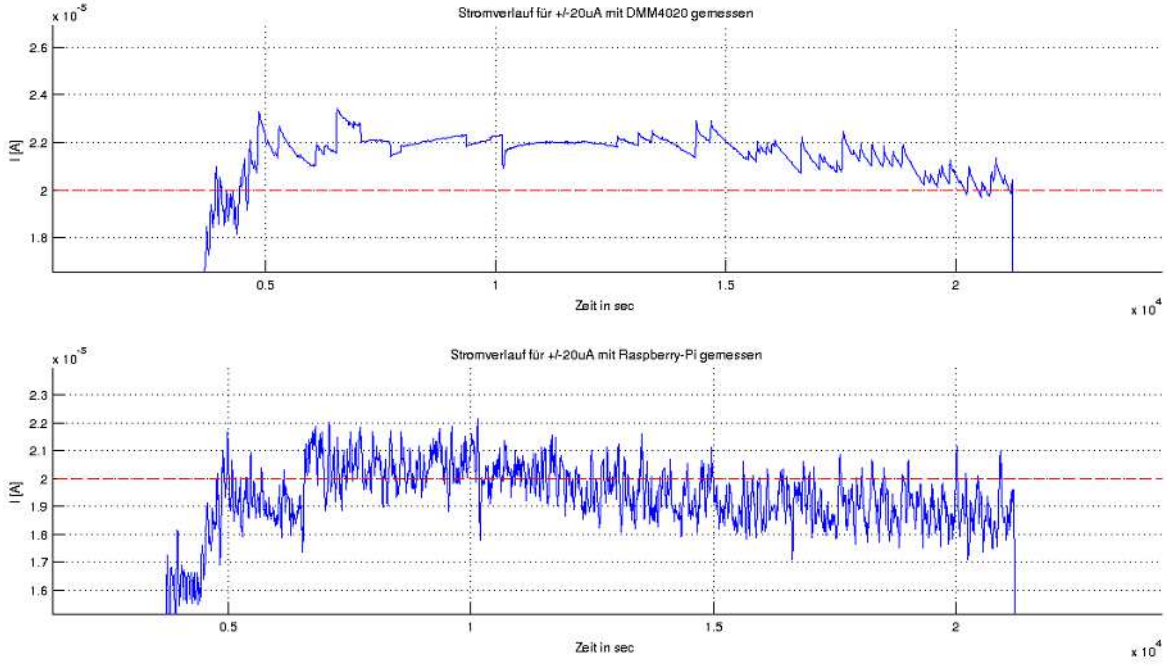

Figure 2.8.: Test charging with 20 μA [3]. Top: measured by Textronix DMM4020 multimeter. Bottom: measured by onboard Ammeter

a) TPS29925 and LD39015, that are supposed to provide 2.5 V and 1.25 V references, are conventional LDO voltage regulators, each with 2% tolerance.

b) There two problem at once concerning the AD7691 ADC is used:

i. AD7691 ADC is a true differential SAR ADC[2] with very narrow common mode input voltage range around $U_{ref}/2$. According to manufacturer violation of this specification degrades the performance of the converter. The way the both ADCs are used leads to such violation. For example let take the ADC in the voltmeter module and assume the battery voltage of 3V (common for lithium batteries). The voltage on positive input of the ADC is the 1.5 (because of voltage divider). Since the negative input is grounded, the common mode voltage is $U_{cm} = (1.5\,\mathrm{V} + 0\,\mathrm{V}/2) = 0.75\,\mathrm{V}$. That presents 0.5 V violation of $U_{ref}/2 = 2.5\,\mathrm{V}/2 = 1.25\,\mathrm{V}$ common mode input voltage specification.

ii. Only positive differential range of the ADCs is utilised, which leads to reduction of the de facto resolution by 1 MSB (from 18 to 17 bit).

c) The OPA743 used in the current regulator module is relatively inaccurate (up to 7 mV input offset voltage) general-purpose operational amplifier and therefore not suitable for a high precision application.

2. Amplification at the instrumentation amplifier in the ammeter module may lead to amplification of noise

3. The layout and routing of the PCB is suboptimal. This includes the reference voltage sources are located far away from the point of their application (Figure 2.9 shows 1.25 V as example).

4. There are many pin headers used for voltage probing and as jumper switches. They may act like antennas and introduce RF interference into sensitive measurement circuit.

5. The decision to use digital potentiometers to control the LED-drivers makes the regulation of luminosity non-linear and thus hard to use. Additionally, the potentiometers have very low accuracy of 1% only.

   This was aggravated by an addtional error [3]: The voltage on the terminal “A” (5V) of the potentiometers must not exceed the digital power supply voltage. However, the latter was set to 3.3 V because it also defines the voltage levels for digital logic. The correction by supplying the “A” terminal with 3.3 V made the required 5V, and thus the complete dimming of the LEDs impossible to achieve.

[2] see section 3.5 for more detailed explanation

6. The capacitor at the output of the TLV2217 3.3V voltage regulator, was too small (1μF) which lead to unstable output voltage. [2]

2.2.1. Implemented Corrections

Some of the problems could be corrected on the existing board with some hot-wiring:

- The output capacitor of the TLV2217 3.3V LDO was increased from 1 μF to 22 μF
- The LD39015 LDO was replaced by LM4121 1.25V reference.
- TPS79925 LDO was replaced with ADR5043 3V shunt voltage reference.
- Additional replacement of passive components as necessary for above listed corrections

S. Pereguda developed a new , more compact PCB layout (Figure 2.10) and made following corrections:

- TPS79925 2.5 V LDO was replaced by AD445BRZ voltage reference.
- LD39015 1.25 LDO was substituted by ADR127 voltage reference.
- TLV2217 3.3 V TO-220 LDO was swapped to ADP151AUJZ-3.3-R7 SMD voltage regulator.

Taking this board in operation is not part this work.

2.3. Definition of Goals for the Redesign

The above described problems necessitate the redesign of the measurement board, and thus gave the motivation for this project. The goals for the redesign are defined as:

- Improve the accuracy and reduce the noise of current regulation
- Improve the accuracy, precision and reduce noise of voltage and current measurement
- Implement hardware changes, where appropriate
- Better implementation of LED control

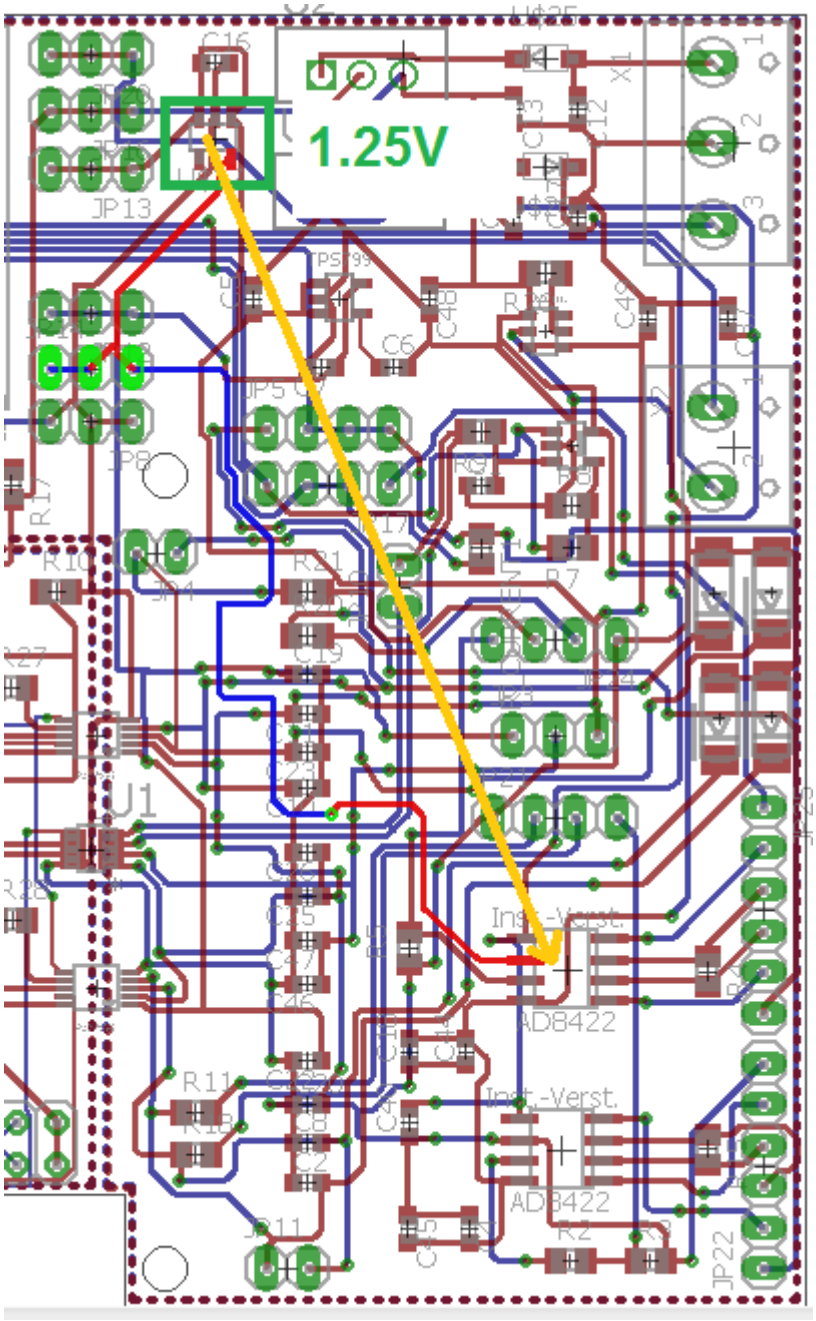

Figure 2.9.: Location of 1.25 V reference relative to the point of the application at the AD8422 instrumentation amplifier, with actual route highlighted

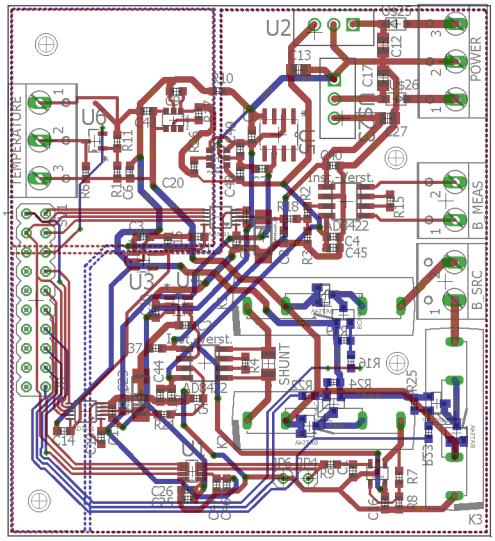

Figure 2.10.: Layout made by S. Pereguda.

- Simplify the design
- Improve the layout and routing of the PCB
- RTC sensor as a ready breakout module

The inclusion of the RTC sensor is a new idea motivated by the fact that Raspberry Pi has no battery backup, which causes the time and date to reset every time the mini PC is switched off. The correct time has to be then set manually or over internet, which may not always be available.

Moreover, it was determined that the temperature sensor would be better connected to Raspberry Pi directly per one-wire interface and therefore does not need support from the board.

Exact specification for the board redesign are given below.

2.3.1. Specification

Table 2.1.: Specification for the redesign of the measurement board

Module	Parameter	Required value	Desired value
Current regulator	Smallest current	±1 μA	±1μA
	Strongest current	±1 mA	±100 mA
	Worst precision and accuracy for current	0.1‰ of strongest current	<0.1‰
	Lowest voltage of discharged battery	1 V	0 V
	Highest voltage of charged battery	4.5 V	6 V
	Precision for battery voltage	50 μV	50 μV
	Accuracy for battery voltage	50 μV	50 μV
	Adjustment rate	50 per second	>50 second
Voltmeter	Lowest voltage at battery	1 V	0 V
	Highest voltage at battery	5 V	6 V
	Accuracy	1 mV	0.1 mV
	Precision	1 mV	0.1 mV
	Largest noise	50 $\mu V_{p\text{-}p}$	50 μV
Ammeter	Smallest current	±1 μA	±1μA
	Strongest current	±1 mA	±100 mA
	Worst precision and accuracy	0.1‰ of strongest current	<0.1‰
	Largest noise	0.1‰ of strongest current	<0.1‰
	Sampling rate	50 SPS	>50 SPS
LED Control	Number of channels	3	3
	Lowest control voltage	0 V	
	Highest control voltage	5 V	
	Type of control signal	PWM or DC	
	Resolution	8 bit	$\geqslant$10 bit
	Control current	μA range	

3. Requirements Analysis and Implementation Decisions

3.1. Discussion of Alternative Concepts for Current Regulation

3.1.1. Limitations of current method

The requirement analysis wouldn't be thorough without considering alternative concepts for current regulator module, especially taking in account limitations of current concept. This concept is a software regulation of current that continually adjusted current based on measured value. However, the software has limited time response making constant current output impossible to achieve. This together with discrete adjustment steps introduces a certain ripple into current. Moreover, it also makes current regulation dependent on accuracy and precision of the current measurements. Additional disadvantage is that the DAC has to cover full range of possible battery voltages, thus further limiting precision of regulation.

3.1.2. Concept for constant current charging

On the other hand there many ways to regulate current in hardware that are able to achieve truly constant current output.One such concept was devised by the author. The idea is to use the reference input of an instrumentation amplifier to introduce an offset relative to the battery voltage, which then causes charging/discharging current (depending on the sign of the offset) to flow over the shunt resistor.

This can be explained in greater detail on basis of Figure 3.1. The battery is modelled as a large capacitor (C1) with an internal resistance (R2). The transfer function of an instrumentation amplifier is $U_{out} = U_{in+} + U_{in-} + U_{ref}$. The easiest connection would be to connect the battery voltage to the positive input of the instrumentation amplifier and ground the negative input. Doing so sets the output voltage of the amplifier to the battery voltage. The high input impedance of the instrumentation

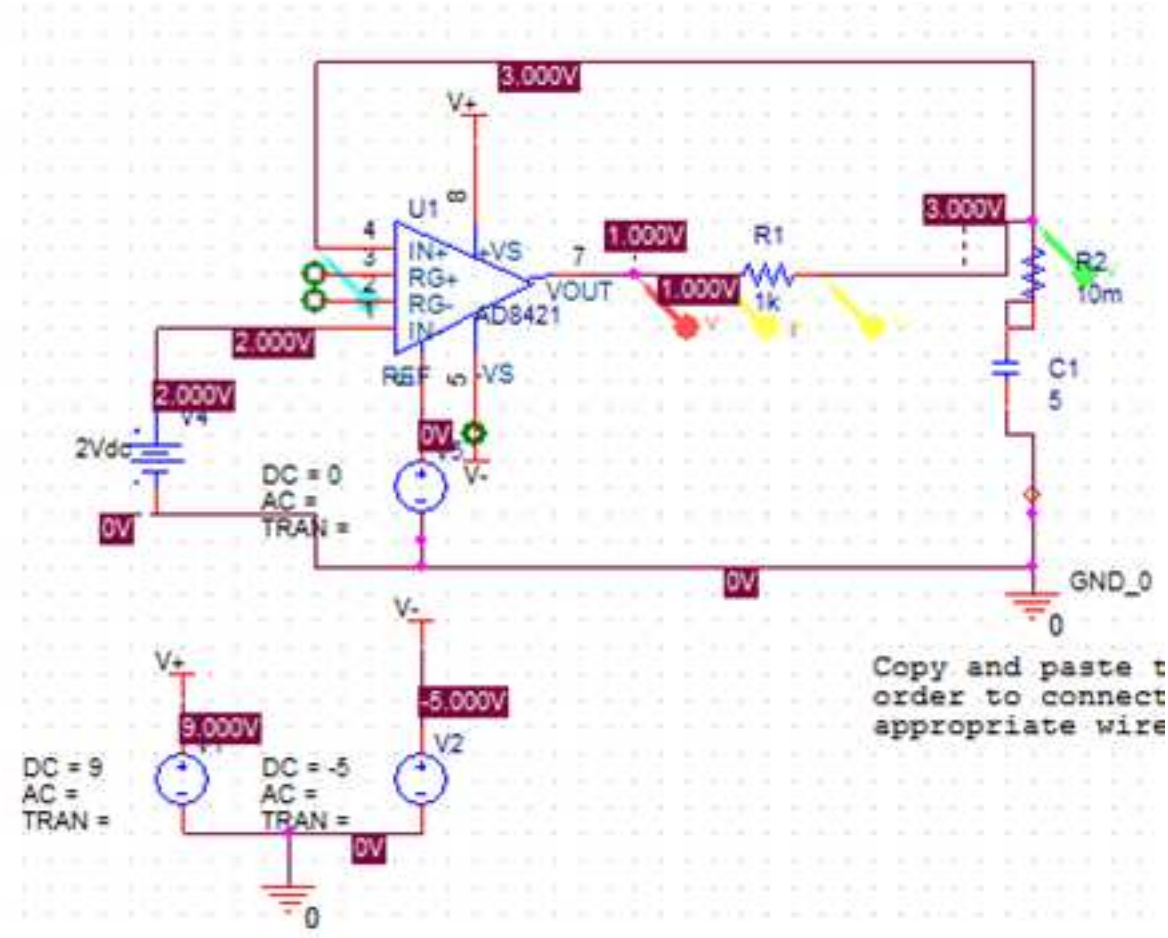

Figure 3.1.: The circuit used for simulation of the constant current concept. The battery is modelled as a large capacitor (5 F) with an internal resistance (10 mΩ). DAC is presented as V5 and the reference voltage as V4

amplifiered ensured that the battery isn't loaded additionally. A DAC, connected to the reference input would be used directly to introduce offset relative the battery voltage and produce current.

However, the disadvantage of a such circuit would be the necessity of the negative voltages at the DAC output. That is why a reference voltage source is attached to the negative input in Figure 3.1 to introduce a fixed negative offset, which the DAC would compensate. The transfer function of the instrumentation amplifier as depicted in Figure 3.1 is

$$U_{out} = U_{bat} - 2\,\mathrm{V} + U_{ref} \tag{3.1}$$

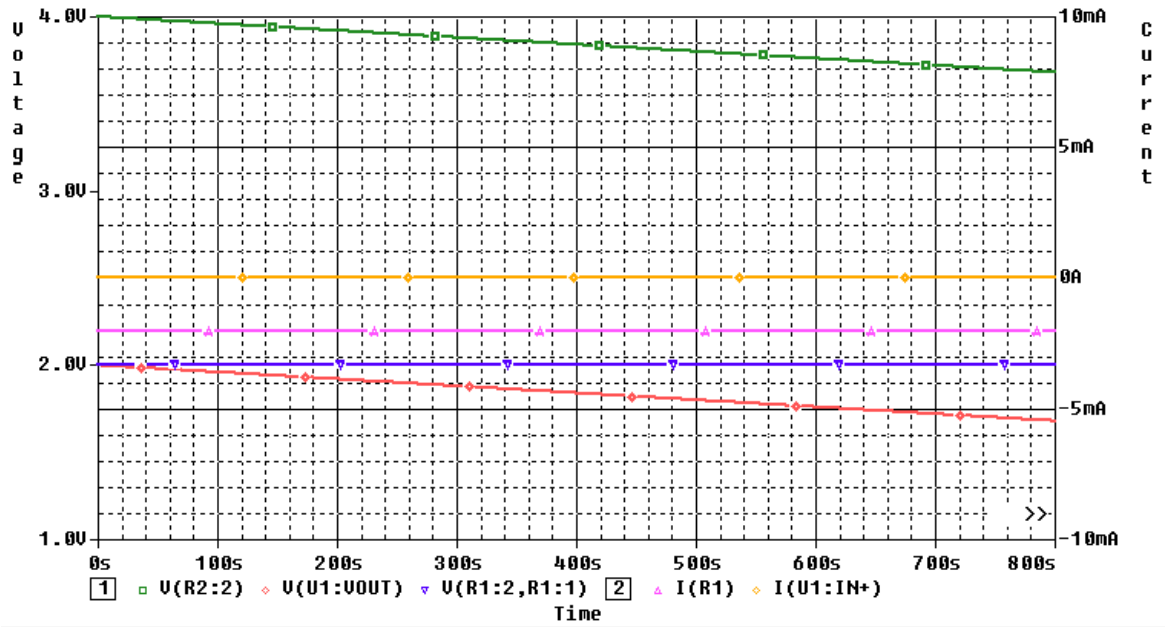

Figure 3.2.: Constant current discharging simulation.
Green: voltage on the battery.
Red: output voltage of the instrumentation amplifier.
Blue: voltage over shunt resistor R1.
Magenta: Current to battery.
Beige: Current into positive input of the instrumentation amplifier

Thereby the introduced offset relative the battery voltage:

$$U_{offset} = U_{DAC} - 2\,\mathrm{V} \tag{3.2}$$

And the charging/discharging current:

$$I_{charging} = \frac{U_{offset}}{R1} = \frac{U_{DAC} - 2\,\mathrm{V}}{R1} \tag{3.3}$$

Thus, the DAC voltage of 0 V correspond to current -2 mA (discharging) and the DAC voltage of 2 V is required to stop the current flow.

The circuit on the Figure 3.1 was simulated in PSpice. The simulation utilized the PSpice model of the AD8421 provided by Analog Devices. The DAC is represented by the voltage source V5 and the voltage reference by the voltage source V4. For discharging (Figure 3.2), the DAC voltage is set to 0 V and voltage on capacitor C1 to 4 V. For discharging (Figure 3.3), the DAC voltage is set to 4 V and voltage on capacitor C1 to 2 V. As the simulation demonstrates, the current stays constant and the voltage on the battery linearly increases or decreases.

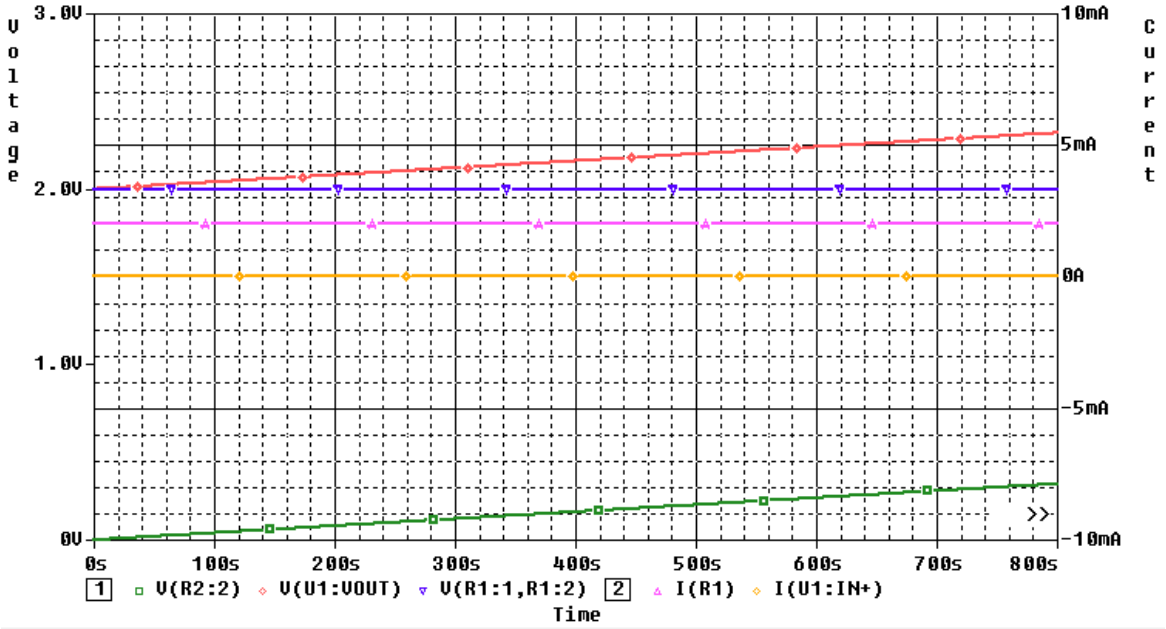

Figure 3.3.: Constant current charging simulation.
Green: voltage on the battery.
Red: output voltage of the instrumentation amplifier.
Blue: voltage over shunt resistor R1 (reversed for better visibility).
Magenta: Current to battery.
Beige: Current into positive input of the instrumentation amplifier

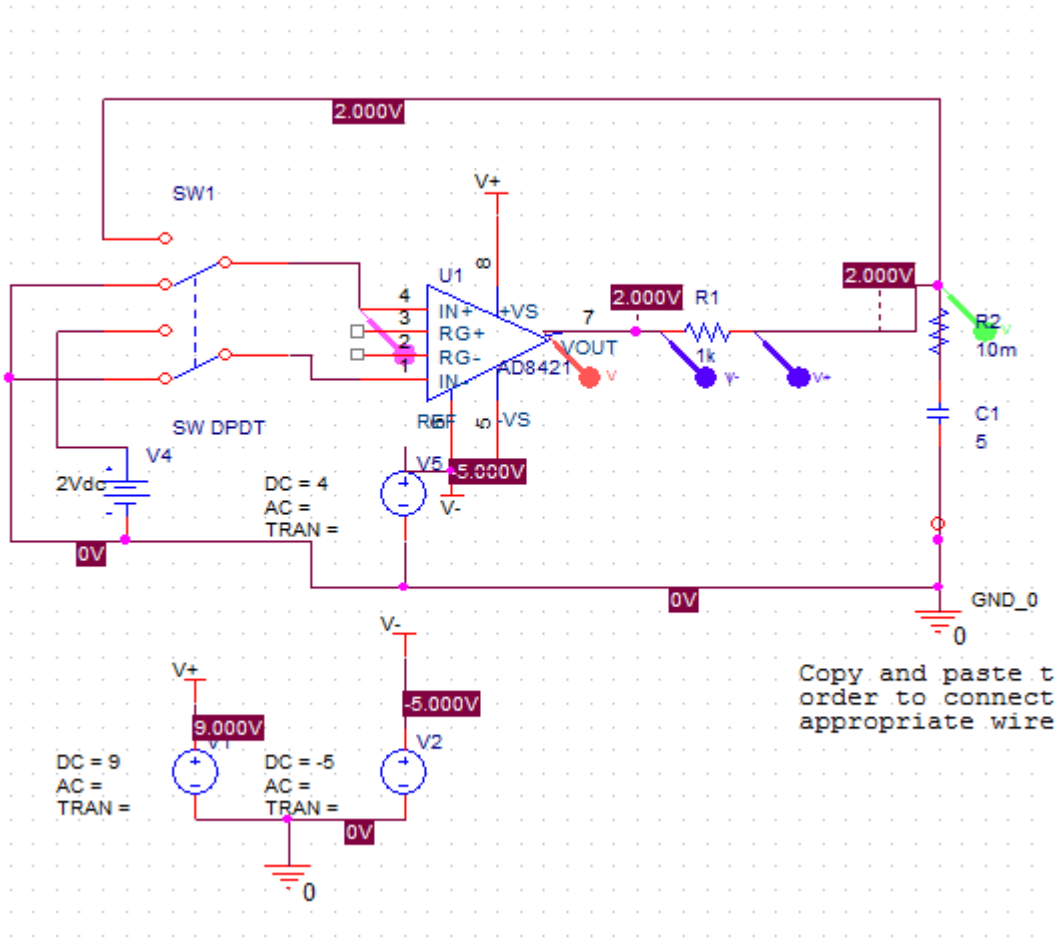

Figure 3.4.: Concept for combined constant current and constant voltage charging and discharging

However, the deficiency of the above presented concept is lack of the constant voltage charging/discharging. The circuit was modified as shown in Figure 3.4. A DPDT switch is used to ground both inputs of the ADC. Thus, the output voltage of the instrumentation amplifier is directly controlled by the DAC. This modified concept was verified by simulation. Since PSpice lacks a time controlled DPDT switch it was modelled by 4 SPST switches (Figure 3.5). The simulation (Figure 3.6) shows the desired behaviour.

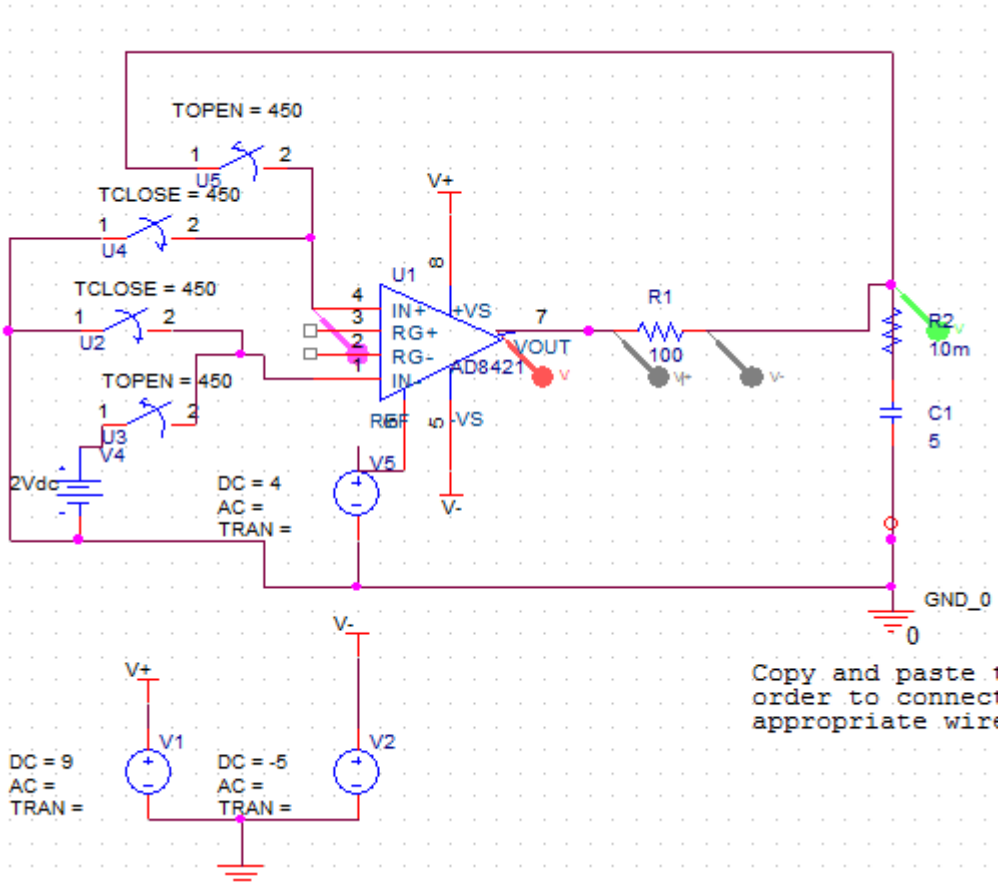

Figure 3.5.: Concept for combined constant current and constant voltage charging and discharging used in the simulation

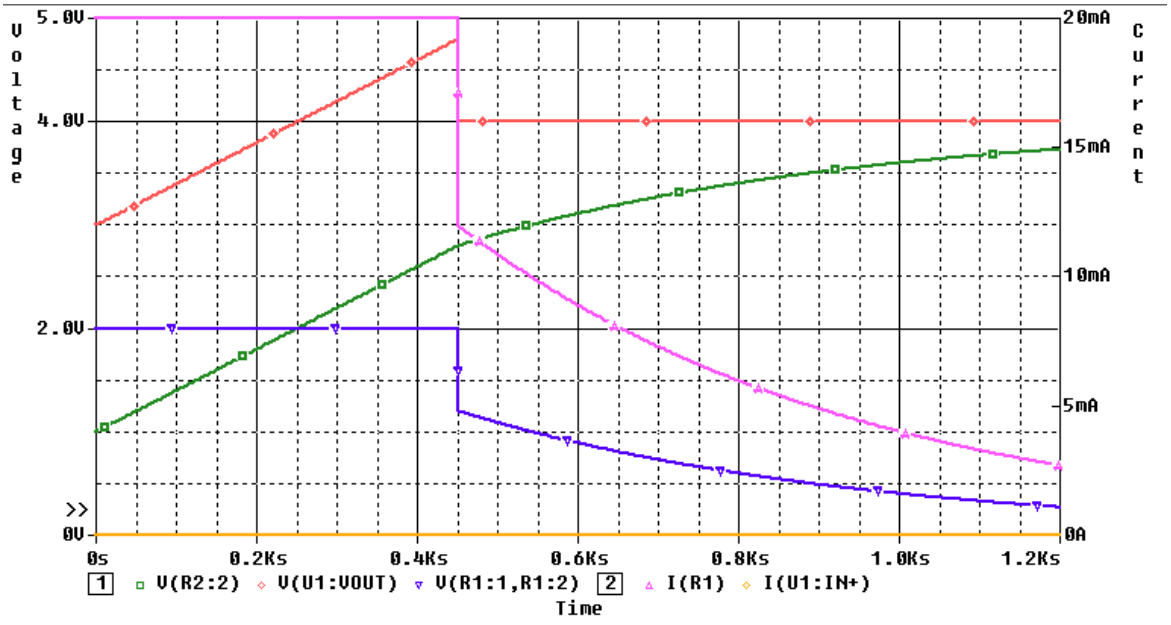

Figure 3.6.: Combined constant current and constant voltage charging. The battery is charged with 20 mA and at time point 450 s is switched to constant voltage charging to 4 V.
Green: voltage on the battery.
Red: output voltage of the instrumentation amplifier.
Blue: voltage over shunt resistor R1 (reversed for better visibility).
Magenta: Current to battery.
Beige: Current into positive input of the instrumentation amplifier

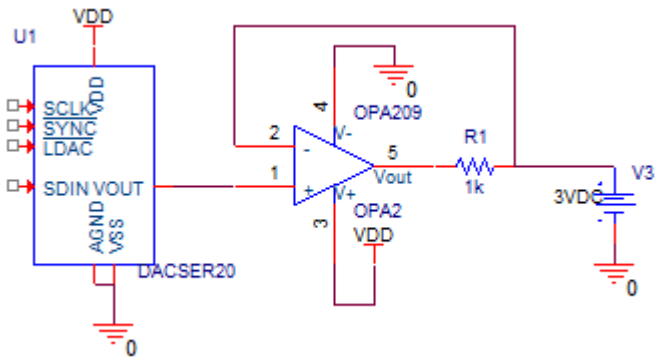

Figure 3.7.: Sergey Pereguda's suggestion for regulation of current. The DAC and operational amplifier are symbolic

3.1.3. Additional Concepts for Hardware Regulation of the Current

There are many more concepts for a controlled hardware regulation of current that, however, weren't studied:

- Transconductance amplifiers with current mirror.[4], [11, p. 943-946]
- Use current output DAC[5].
- An idea by Sergey Pereguda: Figure 3.7
- Voltage controlled current source [4, Figure 10], [6, Figure 4].
- Howland current pump [10].
- Voltage-to-current converter [11, p. 957].
- A few collections of methods to produce current: [7], [8], [9].

3.1.4. Decision about Method of Current Regulation

Sections 3.1.2 and 3.1.3 presented a lot of possible alternatives to current method. However, studying, analysing and testing these options would multiply the required effort and blow the scope of this thesis. That is why the low risk approach, namely attempting to improve on the current concept , was preferred.

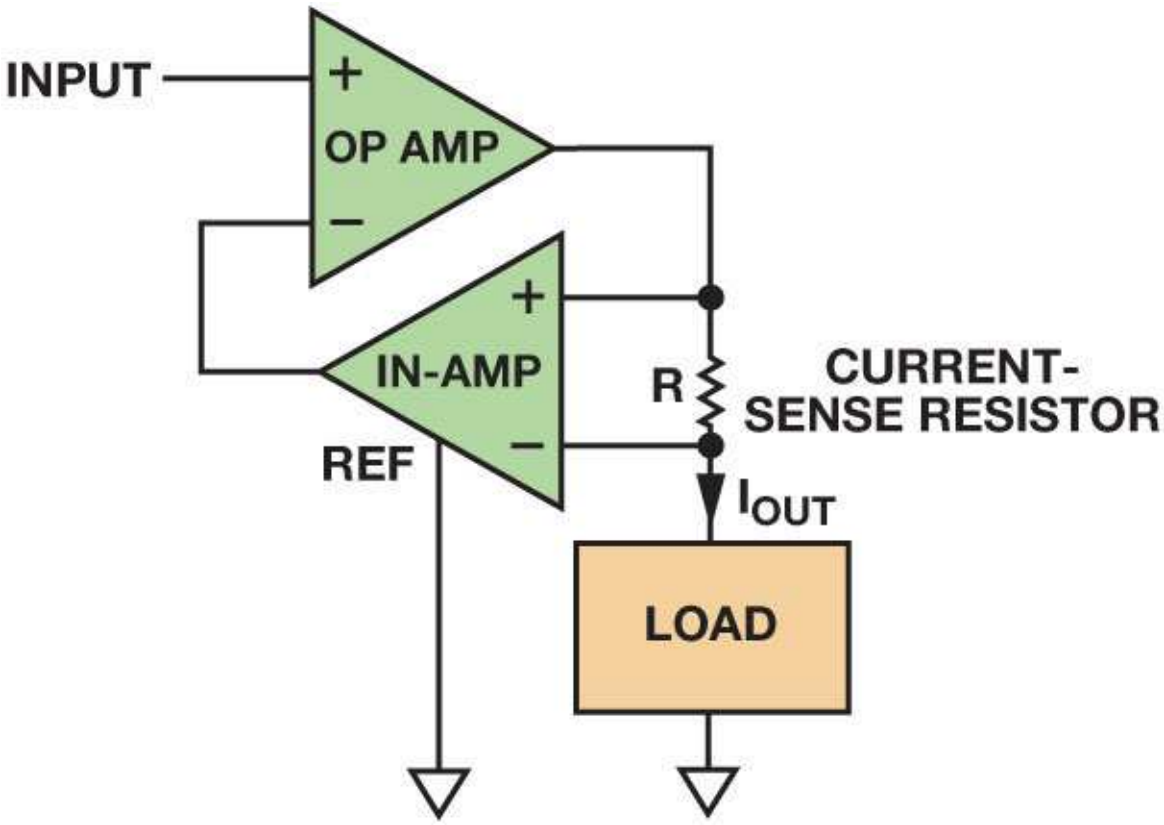

Figure 3.8.: Voltage controlled current source. Taken from [4]

3.2. Sources of Noise and Countermeasures

Given the high requirements for precision of the measurements, it is important to analyse the influence of the noise and develop countermeasures. There are 3 major sources of noise in a measurement system: intrinsic noise of the components, external interference that introduces common mode noise and ADC noise [12][15]. The following subsections deal with the first two of them, while the last one is discussed together with ADCs in Section 3.5.0.1

3.2.1. Introduction to the Intrinsic Noise

3.2.1.1. Basics of Noise Analysis

Intrinsic noise arises due to internal properties of the components and internal processes inside them, like movement of electrons [13]. It is a Gaussian-distributed random process [12][14]. There are several quantities that are used to characterise it:

Noise Spectral Density (NSD) is an empirically determined [12] continuous function that shows the noise contribution at particular frequency given in $\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

RMS noise (V_{rms}) is NSD integrated over a certain bandwidth [14]. It is numerically identical to standard deviation of the noise σ [12].

Peak-to-Peak Noise ($V_{p\text{-}p}$) describes the range of observable noise voltage spikes [13]. In other words it is distance beetween highest and lowest noise value. The way to estimate ($V_{p\text{-}p}$) with V_{rms} is to apply a cresting factor to the latter [12]. Two common factors are used by different sources and component vendors:

- Factor 6 corresponds to 99.7% peak values fall in the specified range [14].
- Factor 6.6 corresponds to 99.9% peak values fall in the specified range [15].

One component that produces noise is a resistor. It is thermal noise, which is white and Gaussian-distributed white. It can be calculated with formula

$$v_n = \sqrt{4kTR\Delta f}$$

where

k is Boltzmann's constant

T is absolute temperature in Kelvin

R is resistance

Δ**f** is bandwidth

In practice, however, a simpler shortcut formula is used to calculate the NSD of a resistance R [12]:

$$\mathrm{NSD}(R) = \sqrt{\frac{R}{1000}} \times 4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$$

For example, a 9000 Ω resistor has a noise spectral density of $\sqrt{\frac{9000}{1000}} \times 4\,\mathrm{nV}/\sqrt{\mathrm{Hz}} = 3 \times 4\,\mathrm{nV}/\sqrt{\mathrm{Hz}} = 12\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

It is important to understand the nois characteristics of linear integrated circuits, like amplifiers, voltage references etc. in order to select suitable component. Such devices typically expose two distinct kind of noise [12][15]:

1/f noise decreases proportionally to frequency. It is usually seen at lower frequencies. The other terms for it are *flicker noise* [13] and *pink noise* [15]. Datasheets often provide V_{rms} in 0.1 Hz to 10 Hz [12] as for 1/f noise reference.

white or broadband noise is uniform at higher frequencies [12][15]. Datasheets usually cite a sample NSD value at a higher frequency as means to provided broadband noise specification.

The transition point from 1/f noise to broadband noise is called *corner frequency* [15]. It can be determined graphically from a chart of the NSD in a datasheet as illustrated by Figure 3.9. Intersil provides free application that can compute noise from parameters and other way round [15].

Current noise presents additional concern in amplifiers because it can be converted to voltage noise by a resistance at the input [12].

The combined contribution from all noise sources can be calculated as geometrical sum of all noise sources [15]:

$$e_n = \sqrt{e_{n1}^2 + e_{n2}^2 + \ldots + e_{nk}^2} \tag{3.4}$$

That is why a single large noise source has dominant contribution [15].

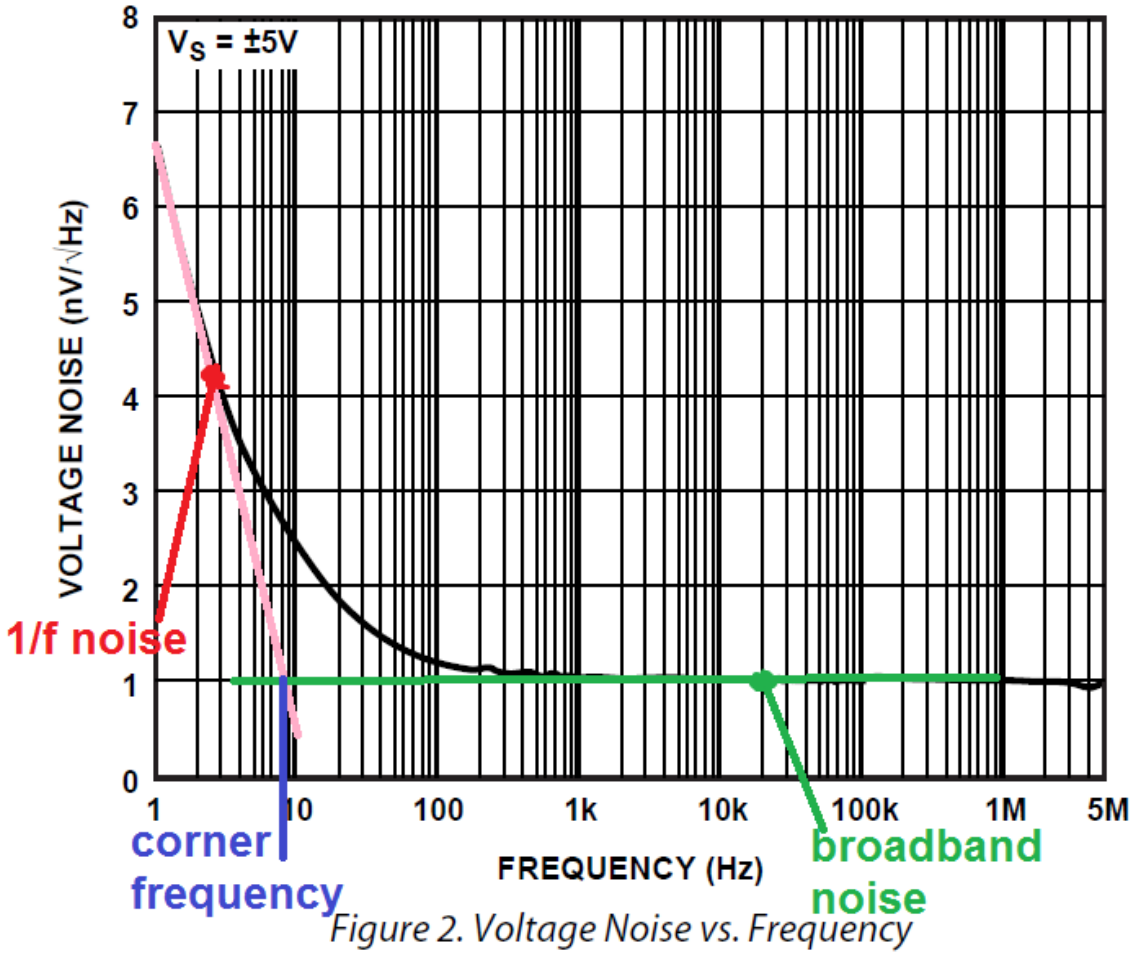

Figure 3.9.: Example of determination of the corner frequency from a noise spectral density chart. Corner frequency of 8 Hz can be deduced from the chart. The 1/f and broadband noise are also marked. Modified from ADA4897 datasheet.

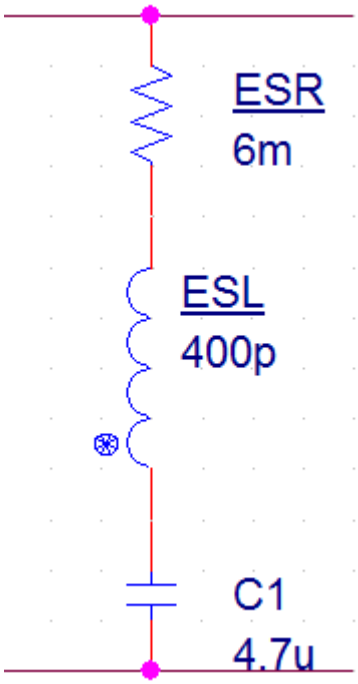

Figure 3.10.: Electric model of a real world capacitor.

3.2.1.2. Noise Countermeasures

One method to reduce noise is selection of low-noise components. Thus, a close attention should be paid to noise specifications.

Another important countermeasure is to utilise *bypass capacitors*, also called *decoupling capacitors*. The way bypass capacitors work to reduce noise can be explained from both frequency domain point of view and from time domain point of view. In frequency domain bypass capacitors shut higher freuqency to ground, while allowing DC current to pass [20]. In time domain they are needed to supply instantaneous current, which may be blocked by parasitic inductance of wires and traces [17][21].

The temperature characteristics of the dielectric of ceramic capacitors must be taken in account. Better dielectrics, like X7R, have more stable capacitance over temperature and operating voltage range [22][23].

Moreover, non-ideal characteristics of the capacitors must be considered for bypass application. That is, capacitors have parasitic resistance, called *equivalent series resistance (ESR)*, and parasitic inductance, called *equivalent series inductance (ESL)* (Figure 3.10) [19][20]. ESL starts to dominate capacitor response at

frequencies higher than *self-resonant frequency* of the capacitor. This can be illustrated by a a simulation in Matlab (Figure B.1).

The first remedy is to place multiple different valued capacitors in parallel that would cover different frequency ranges [21]. The simulation result is shown in Figure B.2. Further improvement can be achieved by using low ESL capacitors in a package with reversed dimensions [22][21]. For example a capacitor in 0306 package has ESL of 111 pH compared to 400 pH in 0603 package. The comparison of their impedance responses is depicted in Figure B.3. The 0306 capacitor demonstrates significantly low impedance at higher frequences.

3-terminal capacitors have exceptionally low ESL and thus are capable to achieve wideband frequency coverage [24]. This is verified by simulation shown in Figure B.4. A single 4.7 μF 3-terminal capacitor is able to cover wide range of frequency with an additional advantage of absence of an impedance spike. Their disadvantage is rather limited choice. There are no capacitors with high operating voltages above 4.7 μF.

Simulation results suggest that three terminal capacitors are highly desirable where the wideband frequency coverage is needed. The second best option, e. g. in case larger capacitance is necessary, is to put a 0306 capacitor in parallel. The latter is also useful for only high frequency bypassing.

3.2.2. Common Mode Noise

Common mode noise is an unwanted signal present on both wires e. g. in a measurement pair [25]. The primary source is external interference such as radio transmission or power lines.

A wide band of common mode noise is to be expected in the measurement environment (see Appendix B.1.2). While the higher frequencies can be suppressed with filtering, it has harder to do for lower frequencies, because it requires large resistors and/or capacitors. This fact necessitates usage of *shielded cable* for measurement connections [26][27]. Making differential measurements either with a differential amplifier or an ADC with differential inputs and high common mode rejection ration can also reduce disturbance due to common mode noise.

3.3. The Roadmap of the Design Process

This section provides insight into the path to final design. The first step is division of the system into hardware modules. Then for each module following steps are performed:

1. Analysis of implementation options. Determination of necessary components, which are highlighted by *emphasis* in appropriate sections. The decision about implementation is dependent on availability of suitable parts and is deferred together with component selection.
2. Definition of requirements for each component. In the sections that perform such definition:
   - *Emphasis* highlight a requirement parameter.
   - Single underscore marks an important intermediate calculations.
   - Double underscore highlights final value of a required parameter.
3. Searching for suitable components:
   a) The web site of retailer of electronic components (like Mouser) are searched through to find out which vendors produce them.
   b) Online catalogues of the vendors are looked for components that satisfy the requirements.
   c) These components go to the list of candidate parts.
4. The candidate components are compared and the most suitable is selected. Simulations are performed if they make sense.
5. An implementation option is chosen with consideration of available parts.
6. The components are procured.
7. The module is assembled on a test board and tested.
8. The test results are analysed and a conclusion is made whether the module satisfies requirements. If not, another implementation option is tested.

3.4. Current Regulator Module

3.4.1. Implementation options

The current regulator has to produce voltage difference relative to the battery in order to induce current flow. With the concept selected in Section 3.1.4 this is accomplished by setting output voltage above or below battery voltage with a *DAC*. This offset together with the dimension of the *shunt resistor* defines the strength of the current. Moreover, since most DACs, including those with built-in buffer, have insufficient current output capability to satisfy the requirements, an *operational amplifier* may be needed to serve as an external buffer. In addition, a relay is nedded to turn current through the battery on and off.

3.4.2. Requirements Definition

The largest allowable size of the voltage offset mentioned in section 3.4.1 has to be established first, because of its significance for the maximum possible strength of the current. On one hand, a larger offset improves the precision for the same value of the maximum current, while on the other hand it reduces the maximum and minimum voltages to which the battery could be respectively charged or discharged. The fact that the highest output voltage of the most DACs is limited to 5 V and the required maximum battery voltage of 4.5 V suggest the highest allowable offset of ±0.5 V. Therefore, the shunt resistance of $R_s = 0.5\,\mathrm{V}/1\,\mathrm{mA} = \underline{\underline{500}}$ is needed to achieve the specified strongest current of 1 mA. Stronger currents can be achieved either by reducing the shunt resistance or increasing the offset at the cost of decreased voltage range of the battery.

The output of the DAC must be able to cover values between the lowest (1 V) and highest battery voltage (4.5 V) plus the above determined offset, which leads to the output voltage range from 0 V to 5 V. The DAC must have *resolution* N that could satisfy the specification (Table 2.1) for precision of voltage and current regulation. The calculation of the resolution with the voltage precision:

$$\begin{aligned} \frac{5\,\mathrm{V}}{2^N} &\leqslant 50\,\mu\mathrm{V} \\ 100000 &\leqslant 2^N \\ N &\geqslant \log_2 100000 \\ N &\geqslant \underline{\underline{16.61\,\mathrm{bits}}} \end{aligned} \tag{3.5}$$

Calculation of the resolution from precision of the current (0.1 ‰ from 1 mA is 100 nA) taking in account the shunt resistance R_s :

$$\begin{aligned} \frac{\frac{5\,\mathrm{V}}{2^N}}{R_s} &\leqslant 100\,\mathrm{nA} \\ \frac{\frac{5\,\mathrm{V}}{2^N}}{500} &\leqslant 100\,\mathrm{nA} \\ \frac{5\,\mathrm{V}}{2^N} &\leqslant 50\,\mu\mathrm{V} \\ 100000 &\leqslant 2^N \\ N &\geqslant \log_2 100000 \\ N &\geqslant \underline{\underline{16.61\,\mathrm{bits}}} \end{aligned} \tag{3.6}$$

Finally, the DAC has to support *SPI interface*.

The buffer operational amplifier has to be low noise in order not to disturb the precision of the measurements. In particular, since the output is essentially DC, the operational amplifier has to have *low 1/f noise* and *corner frequency*. In addition, the *input offset voltage* has to be as low as possible in order to improve accuracy and to reduce variation between different assembled boards. To ensure the necessary output voltage range the *power supply voltage range* in conjunction with *voltage swing to power rails*. Specifically, *RRO*[1] *to negative supply rail* is desirable to avoid the need of negative voltage. Moreover, to guarantee maximum output of 5 V, the operational amplifier has either to possess positive supply rail of $\underline{\underline{5\,\mathrm{V}}}$ and to have *RRO to positive supply rail* or to support supply voltages above 5 V. The *output current capability* has to be as high as possible to enable higher charge/discharge current. At the same time, its *influence on output voltage* has to be taken in account, because higher output currents reduce voltage swing. The resistance of the package has also be taken in account.

3.4.3. Selection of Suitable Parts and Implementation Option

The choice of the DACs with sufficient resolution (18 bits) is rather limited and is listed in Table A.1.

Based on availability of samples only the models by Analog Devices and Maxim Integrated were seriously considered.

One hand the utilisation of the AD5780 and AD5790 would be complicated, because they require negative power supply and high positive supply voltage, as well as an

[1] rail-to-rail output

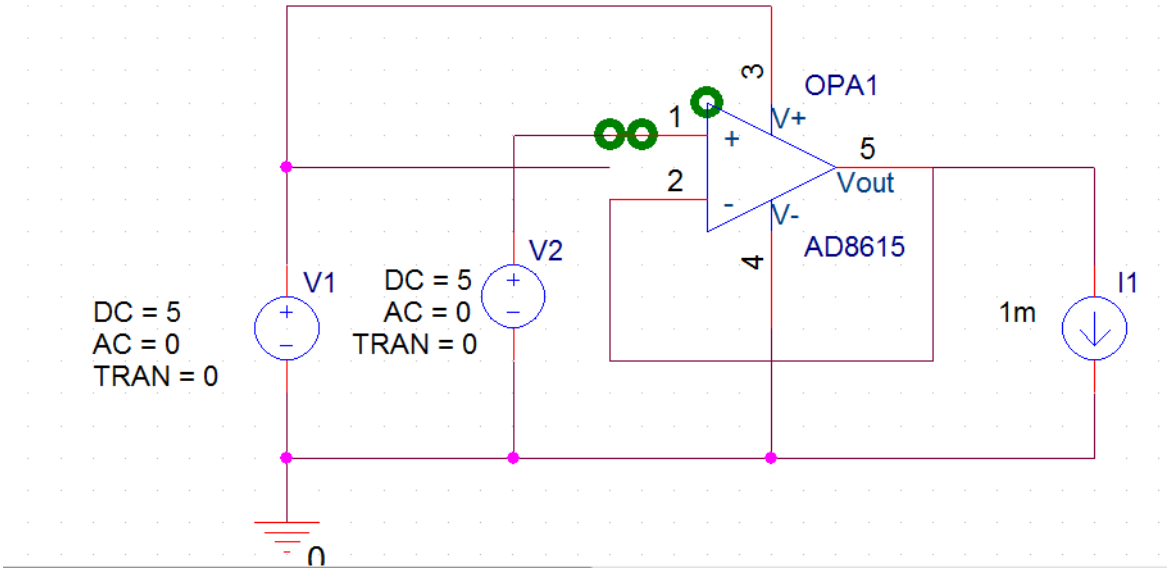

Figure 3.11.: Circuit used in simulation of the operational amplifier current sourcing capability Same circuit was used for other operational amplifiers. The input voltage was set to 0 and current direction reversed in I1.

external buffer amplifier. On the other hand this enables wider output range and thus permits to cover optional battery voltages. In addition, it introduces less noise.

However, the decision was made to make the design as simple as possible, that is why the MAX5318 with its relatively high current integrated buffer was chosen. It has, however, a shortcoming that the input reference voltage is limited to V_{DD}-0.1 V, which would preclude the usage of the necessary 5 V voltage reference with standard 5 V power supply. It can be overcome by applying slightly higher supply voltage. The latter has additional benefit that it increases voltage swing of the output buffer. The details together with the voltage reference that sets the output range of the DAC are discussed in section 3.8.

The above mentioned decision to prefer simplicity eliminated the need of external buffer amplifier. Nevertheless, they are listed in Table A.2 for completeness. The current capability was determined by simulation (Figure 3.11 and Figure 3.12) with the models provided by respective manufacturers. The noise in 0.1 Hz to 100 Hz band was calculated with the tool by Intersil [15].

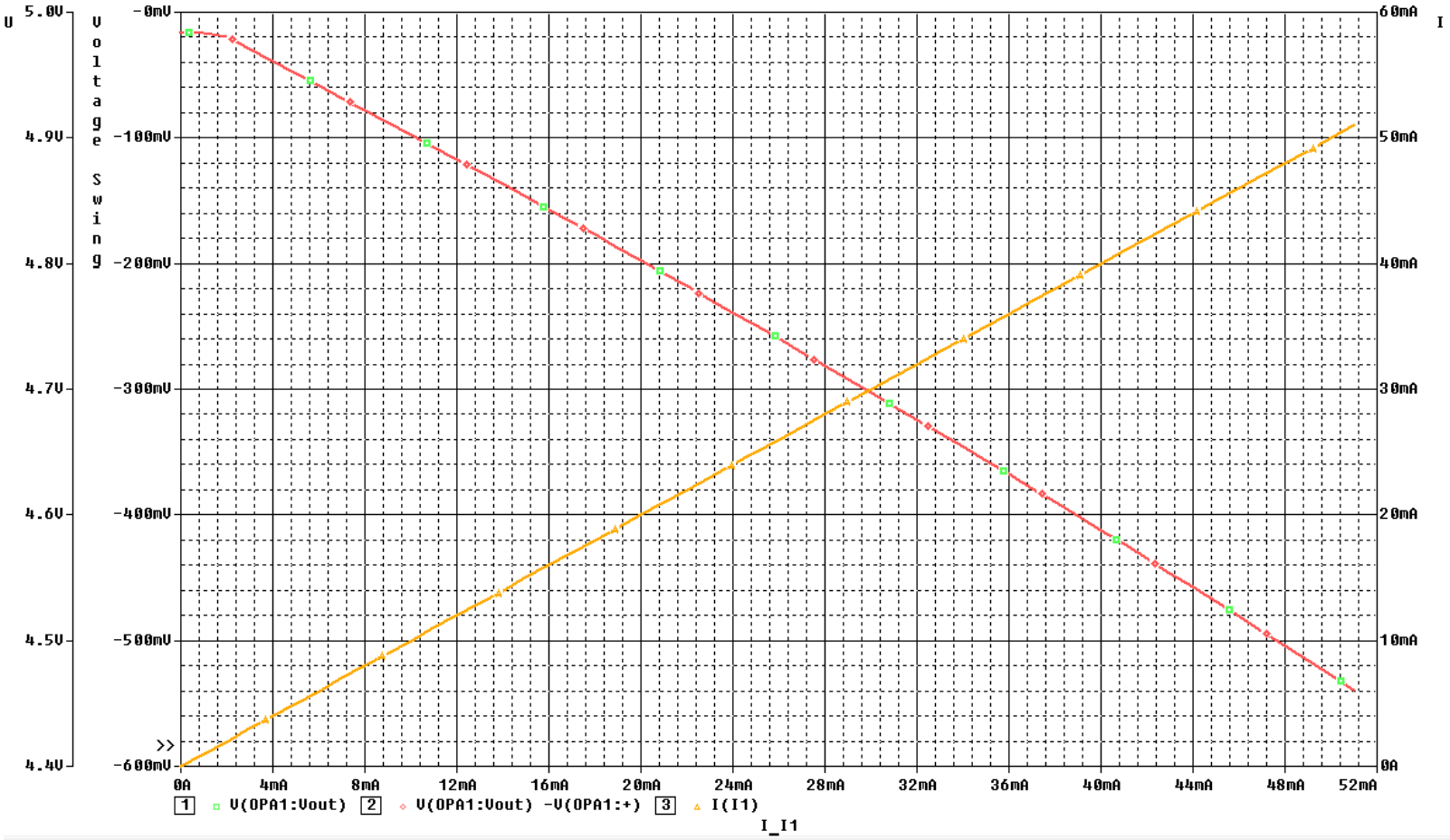

Figure 3.12.: Output of the simulation of the operational amplifer current sourcing capability. Example with AD8615
Light green: output voltage (overlaps with red)
Red: voltage swing (uses different axis)
Beige: sourcing current (right axis)

The AD4897 would be the best choice because of its low noise, high accuracy, overall high voltage swing and availability of samples.

3.4.4. Testing and Conclusion

The summary of the test results comparison with design specification is presented in Table 3.1.

Table 3.1.: Summary of the tests results of the current regulator module. “Strongest current” means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Parameter	**Design Target**	**Acheived**	**Proof**
Weakest current	±1 μA	±1 μA	Ensured by the design
Strongest current	$\geqslant$±1mA	±30 mA	Table B.2, Table B.2, Figure B.13
Worst accuracy for current	0.1‰ of strongest current	Could not be not tested due to lack of constant current regulatioon	
Worst precision for current	0.1‰ of strongest current	$\sim$38 ppm.	Ensured by the LSB of the DAC and shunt resistance
Lowest battery voltage	1 V	1 V- 0.5 V depending on discharging current	ensured by design
Highest battery voltage	4.5 V	4.5 V	Ensured by design
Precision of battery voltage	50 μV	$\sim$20 μV	Ensured by LSB of the DAC
Accuracy if battery voltage	50 μV	$\sim$160 μV	Figure B.9

The current regulator module with MAX5318 at it heart met most design targets. It missed voltage accuracy target due to offset and gain errors. If they are corrected, the targets may be met after all.

3.4.5. Selection of the Relay

A SPST relay is sufficient for switching charging/discharging currents. Optionally a DPST or DPDT[2] relay may be chosen if switching of return current is also desired, which is, however, not the case. Most of SPST relays are of reed type, enumerated in Table A.3. Most relays have either 5 V or low resistance coils and therefore require level shifting in order to be controlled by a GPIO pin. Nevertheless, SIL03-1A72-71D is unique that it possesses a 3 V 500 Ω coil, which results in 6 mA operating current. That is well within current capability (16 mA) of GPIO. Moreover, it has on package flyback diode, and thus safe to operate directly from a GPIO pin of a Raspberry Pi.

This was first verified by a multimeter. Then the relay was installed on prototype board together with the measurement block (Section 3.5.10) and proper operation was confirmed.

3.5. Measuring modules

This section offers introduction to important aspects of analog-to-digital converters (ADCs), which are required for understanding the design decisions for the measurement hardware block. The exact definition of requirements for the ADCs will be done in the following sections.

3.5.0.1. Types of ADCs and ADC Inputs

There are three types of ADC inputs: single-ended, pseudo-differential and (true) differential [28][29]. The single-ended input is the simplest. The input voltage is converted with respect to ground [28][29]. From author's experience they occur only in low resolution ADCs and therefore irrelevant for further discussion.

Differential inputs consist of a positive and a negative input. The ADC converts the voltage difference between them [28]. This gives them a high common mode rejection ratio (CMRR). Differential ADsC are suitable for measurement of voltages over devices, which have both voltage poles floating. In addition, they are usually capable of converting negative differential voltages.

In pseudo-differential inputs the negative input is fixed to a certain voltage, typically ground, that can be used for remote ground sensing [29]. Hence, they are most

[2] capable of switching channels with one switch

suitable for measuring voltages relative to ground, while preserving CMRR of a differential ADC. If the positive input can accept negative voltages, it is called *true bipolar* [29].

The ADCs are often designated by the type of their inputs, Thus, an ADC that has true differential inputs is referred as true differential ADC. The same holds for other input types.

Another important classification of ADCs is according their topology (internal method of performing conversions). The exact functioning of each of them is not important for this work, but only implications for the application. Based of high requirements for measurement precision, and thus the resolution, only two types are worth being considered: successive approximation (SAR) ADCs and delta-sigma (Δ-Σ) ADCs [31].

SAR ADCs have relatively high sampling rate and low conversion latency. However, differential SAR ADCs usually have very limited allowable input common mode range around $U_{ref}/2$ [29].

Delta-sigma ADCs achieve high resolution by oversampling, noise shaping and digital filtering. Yet is done at the cost of low output data rates [30].

Additional features of ADCs may include multiple input channels, integrated voltage references, buffers and amplifiers [31]. Following noise sources are present in an ADC giving it non-ideal characteristics [15]:

Sample jitter arises due to variation of the sample period.

Harmonic distortion is the addition of extra harmonics to the signal. It could be caused by clipping of the signal at the supply rails in an ADC driver amplifier.

Inter-modulation distortion is harmonic distortion resulted from mixing signals of different frequencies and caused by non-linear behaviour of the signal processing.

Quantization noise is the noise introduced by quantization error, which in turn is difference between input and discrete output of the ADC

Analog noise, (code) transition noise, input-referred noise originates from the fluctuating threshold for code transition. The cause is resistor and semiconductor noise [34].

Sample jitter, harmonic distortion and quantization are of importance only for time-varying signals. Since the measurements to be performed are DC, the first two are irrelevant and can be neglected. The latter is insofar significant that the smallest quantisation step (*least significant bit (LSB)*) sets the lower bound for the precision of the measurement.

The analog noise, reinforced by external noise sources, is present even at DC [34]. Thus, it is the main noise component.

Noise can be specified in root-mean-square Volts or peak-to-peak Volts [33] or in equivalent LSBs. SNR (signal-to-noise ratio), a popular criterion of ADC performance is defined as [15]

$$SNR = 20 \lg \left(\frac{U_{input}}{U_{RMSnoise}} \right) \tag{3.7}$$

Similar parameter is SINAD (signal-to-noise and distortion ratio), which takes in account all noise sources listed in the beginning of this section.

Noise induces the reduction of real resolution relative to the nominal one. Their are several quantities in relation to it. *Effective noise* is the ratio of the full-scale range at nominal resolution N to the RMS input noise [34]:

$$Effectiveresolution = \log_2 \left(\frac{2^N}{RMS\ noise\ (LSBs)} \right) \tag{3.8}$$

Effective number of bits (ENOB) is calculated from SINAD [33].

Another useful quantity is *noise-free (also called flicker-free) resolution* [34] that presents number of bits that stays stable at a given input level. It is specified as binary logarithm of the ratio between fullscale and number of output codes, called *counts*:

$$Noise\text{-}free\ resolution = \log_2 \left(\frac{2^N}{peak\text{-}to\text{-}peak\ noise\ (LSBs)} \right) \tag{3.9}$$

$$= N - \log_2(peak\text{-}to\text{-}peak\ noise\ (LSBs)) \tag{3.10}$$

3.5.1. Implementation Options of the Ammeter

The ammeter has to measure the current through the battery. The best option is to utilise a *fully differential ADC* to directly measure the difference between DAC and battery voltages over the shunt resistor. Since the measured currents are quite low (down to µA range), a *high input impedance buffer* is needed in order not to distort the measurement. Ideally, the ADC itself would have such a buffer built in.

Additional possibility is to use an *instrumentation amplifier* to get voltage over shunt resistor. This would be similar to the previous implementation . The difference is that a *bipolar pseudo-differential ADC* would be used to digitize the output of the instrumentation amplifier. A major disadvantage of this option is the need for negative power supply. On the other hand it allows for wider range of measurable DAC and battery voltages, and would be implemented in case of the voltages that exceed input range of typical ADCs.

3.5.2. Requirements Definition for the Ammeter

The analog inputs of the fully differential ADC must be able to sustain full output range of the DAC (0 V to 5 V). As established in Section 3.4.1, the usual differential voltage is ±0.5 V. However it would be prudent to provide for higher voltages in case the option for higher currents is used. In addition, the ADC has to support DC common-mode voltage between 0 V to 5 V that disqualifies most successive approximation ADCs (see Section 3.5.0.1) and leaves delta-sigma ADCs.

The buffer amplifier must not load battery. Hence, it must feature high impedance inputs and low bias currents. In order not to disturb the measurement, it must be as low noise and high DC accuracy as it can possibly get. Also has to support input voltages between 0 and 5 V.

The instrumentation amplifier option must support full output voltage range of the DAC. It must be capable of output of voltage difference over the shunt resistor of at least ±0.5 V. The pseudo-differential ADC must in turn feature true bipolar input that support this voltag range.

The calculation of resolution requirements N for ADCs for both options is the same and depends from voltage reference that would set the fullscale. Ideally, it would cover the bipolar range of ±0.5 V results in total span of 1 V.

$$\begin{aligned} \frac{\frac{1\,\mathrm{V}}{2^N}}{R_s} &\leqslant 100\,\mathrm{nA} \\ \frac{\frac{1\,\mathrm{V}}{2^N}}{500} &\leqslant 100\,\mathrm{nA} \\ \frac{1\,\mathrm{V}}{2^N} &\leqslant 50\,\mu\mathrm{V} \\ 20000 &\leqslant 2^N \\ N &\geqslant \log_2 20000 \\ N &\geqslant \underline{14.29\,\mathrm{bits}} \end{aligned} \tag{3.11}$$

If the reference is higher voltage, the fullscale expands and required resolution rises.

3.5.3. Selection of Suitable Parts for Ammeter

The candidate ADCs for the ammeter block are listed in Table A.4. All DACs are of Δ-Σ type and feature 24 bit nominal resolution. Only those with internal oscillator were taken in consideration.

Since there are few options with a usable internal buffer, the ADA4522 could be used. It leaves nothing else to desire with very low noise (5.8 nV/$\sqrt{\text{Hz}}$), absent flicker noise, low offset voltage (2.5 μV), wide supply voltage range of 55 V, low input bias currents (50 pA) and rail-to-rail output capability.

Since the support of extended battery voltages deemed to be unnecessary, the instrumentation amplifier implementation option was not considered. Morever, the combined ammeter/voltmer described in Section 3.5.7 was preferred because of its simplicity.

3.5.4. Implementation Options of the Voltmeter

The voltmeter has to perform remote measurement of the voltage over the battery. The easiest option would be to measure voltage at the battery terminal of the shunt resistor. However, this would lead to inaccuracies due to the voltage drop over the wire produced by charging and discharging currents.

That is why it is best to use a separate pair of wires for 4-wire sensing. A *pseudo-differential ADC* would be excellent as it allows the remote sensing of the ground. The voltage drop has to be eliminated as best as possible for the maximum accuracy by utilising high input impedance buffers. These would be ideally integrated directly into the ADC. It also has to support SPI interface

3.5.5. Requirements Definition of the Voltmeter

The pseudo-differential ADC has to be capable of measuring unipolar voltages at least between 1 V and 4.5 V.

Considering that the closest suitable voltage references are 5 V and taking the optional specification for precision of 0.1 mV the necessary resolution N can be calculated as following:

$$\begin{aligned} \frac{5\,\text{V}}{2^N} &\leqslant 0.1\,\text{mV} \\ 50000 &\leqslant 2^N \\ N &\geqslant \log_2 50000 \\ N &\geqslant \textit{15.6 bits} \end{aligned} \tag{3.12}$$

The requirement for buffer is similar to those for the Ammeter.

3.5.6. Selection of Suitable Parts for Voltmeter

The candidate ADCs for the ammeter block are listed in Table A.5. All presented ADCs are 18 bit SAR.

The ADA4522 would be excellent choice as the input buffer for the reasons listed in Section 3.5.3. Yet again the decision was made to prefer simplicity that is why a combined ammeter/voltmer described in Section 3.5.7 was favoured implementation.

3.5.7. Combined Voltmeter and Ammeter

One more possible implementation of the ammeter and the voltmeter is to combine them by means of a shared *multichannel ADC*. The advantage is simplification of the circuit. This comes at price that both the ammeter and the voltmeter are forced to operate in the same fullscale range, which would be not optimal for both of them. The ammeter has differential ±0.5V to ±1 V optimal range, (Section 3.5.2), while the voltmeter has 5 V unipolar range (Section 3.5.4). Therefore, in order to accommodate both requirements the ADC has to have *±5 V differential range*, which gives fullscale of 10 V. This means that 8 V to 9 V of the span are wasted from the perspective the ammeter, while the voltage measurement, which would be performed pseudo-differentially, would not utilise a half of the ADC span losing 1 bit of resolution. The ADC, which must have at least *two differential inputs*, has to be of the *delta-sigma architecture* for the reason stated in Section 3.5.2.

3.5.8. Selection of Suitable Parts for the Combined Ammeter/Voltmeter

The combined ammeter/voltmeter option was nevertheless chosen for implementation, because the simplification it offers prevailed over its deficits mentioned in the Section 3.5.7. In addition, the typically high resolution (24 bit) of delta-sigma ADCs can perhaps compensate for the shortcomings. However, this has to be verified by calculation.

The theoretical precision of the voltage measurement:

$$\frac{10\,\mathrm{V}}{2^{24}} = 596\,\mathrm{nV} \tag{3.13}$$

The theoretical precision of the current measurement:

$$\frac{\frac{10\,\mathrm{V}}{2^{24}}}{500} = 1.19\,\mathrm{nA} \tag{3.14}$$

The minimum resolution that required to meet specification for voltage (16.6 bit) and current (17.6 bit) accuracy at fullscale of 10 V can be calculated like in Equations 3.11 and 3.12.

The multichannel $\triangle$-ΣADCs for the united measurement module is presented in Table A.6. AD7175-2 was chosen from them. Although its higher data rates are not needed, at the same time it has lower noise and higher effective resolution at lower output data rates than AD7172-2. On the end, the AD7177-2 has only marginal advantage at minimal ODR.

3.5.9. Reduction of Noise

This section applies theoretical findings from Section 3.2, and discusses concrete ideas for noise reduction.

The first one is to make sure that the ADc is properly bypassed. The recommendations from the data sheet has to be followed.

Then the addition of the input filters would serve bandlimiting external noise. The delta-sigma ADCs have rather relaxed requirements for input filters, so a passive first order filters totally suffices [35].

An input filter consist of differential mode (Figure 3.13) and common mode filters (Figure 3.14)that act on matching types of noise [36]. Since the differential signal is the one that gets converted in a differential ADC, the corresponding filter is crucial. The first step in designing it is the selection of the cut off frequency. Since the measurement are DC, it should be ideally 0, which is impractical. So based on probable noise sources identified in Section 3.2 it is a good idea to set the cut off frequency to 50 Hz power line frequency. Now we need to determine the values of resistors and the capacitor. 4.7 μF is one of the highest capacitor values that comes at reasonable size. The calculation of the resistor value [36]:

$$\begin{aligned} f_C &= \frac{1}{2\pi \times 2R \times C_{diff}} \\ R &= \frac{1}{2\pi \times f_C \times 2C_{diff}} \\ R &= \frac{1}{2\pi \times 50\,\mathrm{Hz} \times 2 \times 4.7 \times 10^{-}6\,\mathrm{F}} \\ R &= 338.6 \end{aligned} \tag{3.15}$$

Such relatively large resistor could potentially cause measurement inaccuracy due to voltage drop that, however, can be mitigated by enabling internal input buffers.

Ideally CMRR of a differential ADC would take care of common mode noise. Still large amount of noise could saturate the inputs and thus overwhelm CMRR, making a common mode filter desirable. The drawback is that the tolerances of passive components will convert a certain mount of common mode noise to differential signal. Luckily, this additional noise fill be blocked by the differential mode filter if the cut off of the common mode filter is at least tenfold of differential cut off [36]. 4.8 kHz was chosen because it can be build with ubiquitous 100 nF capacitors.

$$\frac{1}{2\pi \times 100\,\mathrm{nF} \times 330\,\Omega} \approx 4822\,\mathrm{Hz}$$

Unfortunately, such relatively high cut off passes low frequency common mode noise, making shielding necessary [37].

Shielded cables usually come as twisted pairs or bundles. There two types of shield: braid and foil [38]. The (aluminium) foil offers full coverage, while (copper) braid has features lower resistance. The latter property is more important for low frequencies [39], therefore a braided cable was selected.

3.5.10. Testing the ADC and Decision

The results of the tests are summed up Table 3.2

Table 3.2.: Summary of the tests results of the measurement module. “Strongest current” means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Function	Parameter	Design Target	Achieved	Proof
Voltmeter	Lowest voltage at battery	1 V	0 V	Ensured by design
	Highest voltage at battery	5 V	5 V	Ensured by design
	Accuracy	1 mV	70 μV?	Figure B.31, Figure B.30. However, unreliable due to low precision of digital multimeters.

Table 3.2.: Summary of the tests results of the measurement module. “Strongest current” means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Function	Parameter	Design Target	Achieved	Proof
	Precision	1 mV	300 nV	Ensured by the LSB of the
	Largest noise	50 $\mu V_{p\text{-}p}$	15 $\mu V_{p\text{-}p}$	Figure B.18
Ammeter	Smallest current	±1 μA	±1 μ	Ensured by design
	Strongest current	±1 mA	±30 mA	Ensured by design. See also Section 3.9.1
	Worst accuracy	0.1‰ of strongest current	50 ppm after self-calibration	Figure B.28
	Worst precision	0.1‰ of strongest current	1.2 ppm with external reference, 0.6 ppm with internal reference	Garanteed by LSB and shunt resistance of the ADC. Equation 3.14
	Largest noise	0.1‰ of strongest current	7 ppm	Figure B.21, Figure B.22
	Sampling rate	50 SPS	100 SPS, 50 SPS for Voltmeter and Ammeter	Supported by the ADC

The ADC presented promising performance overall, especially considering rather crude prototype assembly. All design targets were met. An improvement in performance may be achieved with a properly implemented PCB design that, however, has to be verified then.

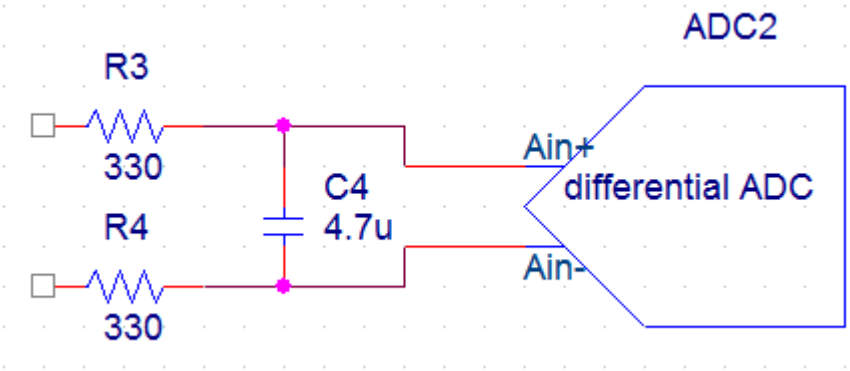

Figure 3.13.: Example of a differential mode filter

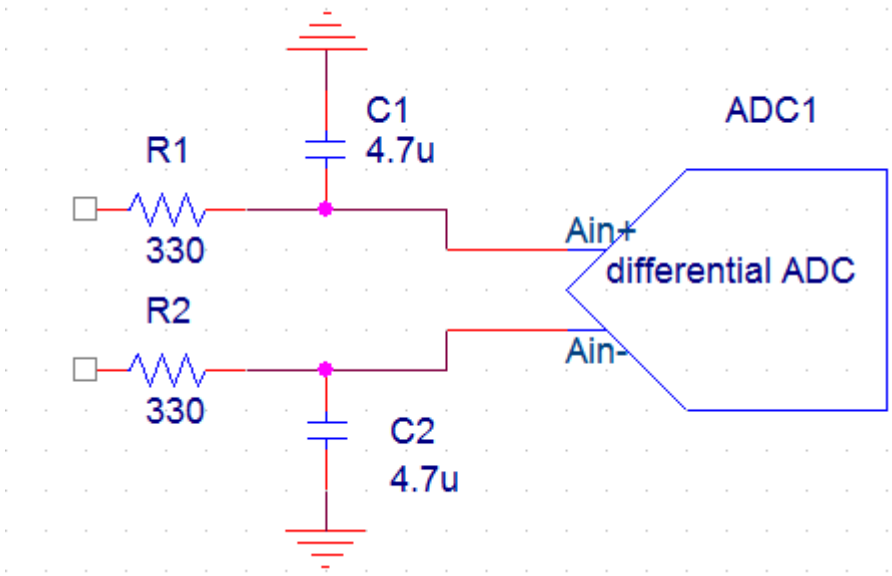

Figure 3.14.: Example of a common mode filter

3.6. LED Control

3.6.1. Implemention Options and Requirements Definition

The LED drivers accept either a PWM or DC signal in a range of from 0 V to 5 V (Table 2.1). The first option could be controlling LED drivers directly from Raspberry Pi with PWM. However, Raspberry Pi has only 2 PWM channels, which are insufficient. The other option is to control the drivers with a DC voltage from a *multichannel DAC*. The DAC has to have at least 3 output channels and support voltages from 0 V to 5 V.

3.6.2. Selection of Suitable Components

Since there are no strict or special requirements for the DAC, there are a lot of suitable models from different vendors. AD5684 12 bit 4-channel DAC by Analog Devices was selected because availability of samples. An alternative could be the AD5684R variety with built-in voltage reference. The arguments in favour of each part are listed below:

- Advantages of an AD5684 with external reference: Lower noise and better temperature coefficient
- Advantages of an AD5684R: simpler, saves routing and a bypass capacitor

Given the absence of special requirements for noise, the AD5864R was selected for testing for simplicity if implementation.

The internal reference is 2.5 V. Nonetheless, the gain of the output buffers can be set to 2 producing required 5 V.

3.6.3. Decision

Table 3.3.: Comparison of the specification with capabilities of AD5684R.

Parameter	**Specification**	**AD5684R**
Number of channels	3	4
Lowest control voltage	0 V	0 V

Table 3.3.: Comparison of the specification with capabilities of AD5684R.

Parameter	**Specification**	**AD5684R**
Highest control voltage	5 V	5 V, achieved by internal 2.5 V reference with output buffer gain of 2
Type of control signal	PWM or DC	DC
Resolution	8 bit	12 bit
Control current	μA range	mA range

The AD5684R fulfils specification and can be used in LED control module. The testing is described in Appendix B.4.

3.7. Real-Time Clock

The RTC has to support the *SPI interface*. It can be built either on the board or acquired as a prebuilt break out board.

Two RTC ICs that support SPI are available on the market: DS1302 and DS3234. DS1302 is cheaper, but DS3234 is more accurate and temperature compensated.

It turned out that DS1302 support SPI in half duplex mode only, which is unacceptable. That left DS3234 woithout competition.

DS3234 was tested on a premanufactured break out board. It could be set to the system time as well the system time could be reset from it. This module has low priority and wasn't invested that much.

3.8. Power Supply and Voltage Reference

Now after all active components are known, power supply requirements can be determined. The voltage levels and current requirements are listed in Table 3.4. As can be seen from the table the design goes without negative voltages. The number of voltage levels is reduced too compared to previous design. Now we consider possibilities to implement them. Although there are plenty of fixed 5 V LDOs, there are three compelling reasons to raise supply voltage above 5 V, as close as possible to the operational maximum of 5.5 V:

Table 3.4.: Power supply requirements

Voltage level	Device	Purpose	Max. operating voltage, V	Max. current draw, mA
⩾5 V Analog	MAX5318	AVDD	5.5	6.5
		Charging current	5.5	30
	AD7175-2	AVDD1	5.5	16
		AVDD2	5.5	5.2
	AD5684R	VDD	5.5	1.3
	Total			**59**
5 V Reference	MAX5318		5	0
	AD7175-2		5	0.001
	Total			**0.001**
3.3 V digital	MAX5318	VDDIO		0.005
	AD7175-2	IOVDD		3.1
	AD5684R	VLogic		0.03
	DS3234	VCC	5.5	0.4
	Total			**3.408**
Overall total				**62.509**

1. Circumvent Vdd-0.1 reference voltage limitation of MAX5318. Otherwise it would not be possible to use 5 V reference.
2. It also increase the linear range and current sourcing capability of the internal buffer of MAX5318.
3. It can provide a neccessary low voltage drop for the voltage reference. Otherwise an additional higher voltage level would become necessary just to supply the voltage reference.

LT3042 (Table A.7) was chosen because of excellent accuracy and exceptionally low noise.

As for reference, LT6655B was selected (see Table A.8) for its high accuracy very low noise and low temperature coefficient.

The 3.3 V is required to supply digital interfaces of the data converters. It also sets logic levels for communication. The easiest option is simply source it from Raspberry Pi, which also ensures proper logic levels .

An external 9 V linear regulated power supply unit is to provide the main power to the board. The LDO regulator was put in operation during both DAC and ADC test.

Even during highest current draining (e. g. during DAC current capability test) it remained stable and without palpable heating.

3.9. Passive Components

While in most cases generic passive components are sufficient, some hardware modules have special requirements. The most important of them are shunt resistors for current regulator.

3.9.1. Shunt Resistor Network

Accuracy of current measurement and regulation is dependent on shunt. Therefore precision 0.1% 500 Ω KOA-Speer RN732ATTD5000B25 was acquired for this role.

Moreover, since the DAC is capable of higher output current, it is highly desirable to provide support for it to satisfy extended specification. This is done by lowering shunt resistance. It would be good to provide different options for battery current without a need for resistor replacement. This could be accomplish by putting additional resistors varying their connection. Three 50 Ω resistors are particularly favourable because following combinations of them are possible:

Table 3.5.: Possible combinations of three 50 Ω shunt resistors and corresponding maximum battery currents

Resistor connection, R=50Ω	**Resistance, Ω**	**Strongest current, mA**
3R	150	3.33
2R	100	5
R	50	10
2R||R	33.3	15
R||R	25	20
R||R||R	16.6	30

Of course, these resistors must be accurate too, that is why Vishay TNPW120650R0BEEN07 were obtained. They have 0.1% tolerance and 25 ppm temperature coefficient while remaining affordable.

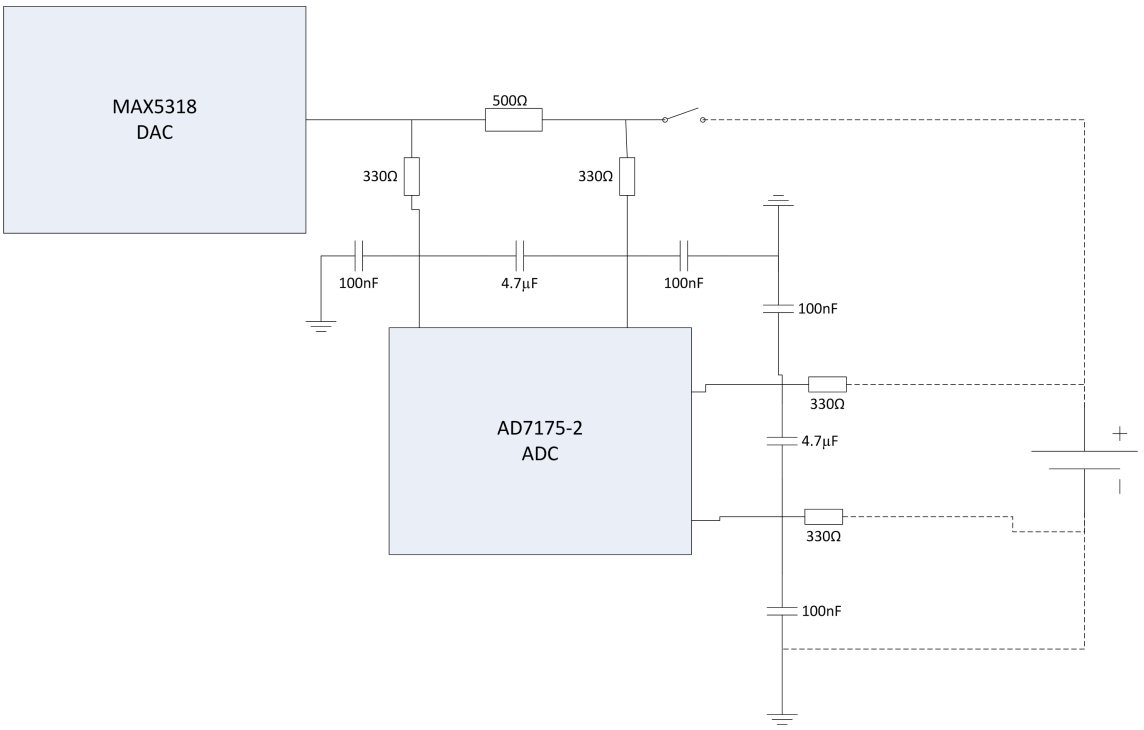

Figure 3.15.: Block diagram of current regulating and measuring system.

3.9.2. Voltage Setting Resistor

The output voltage LT3042 of LDO is set with a resistor according to formula

$$U_{out} = 100\,\mu\text{A} \cdot R_{SET}$$

Therefore, in order to achieve voltage close to 5.5 V (see Section 3.8) a 54.9 kΩ resistor could be used. However, the tolerances of 1% could cause the LDO voltage to exceed 5.5 V, which is undesirable. Therefore a resistor with a better tolerance is necessary. That is why Yageo RT0805BRD0754K9L 0.1% was picked up.

3.10. Overview

The new design succeeded in significant simplification of the design. That is, the number of components was reduced relative to previous design and power supply was simplified. The block diagram of the system created during current design process is depicted in Figure 3.15 The testing showed promising results and presents a well defined concept for the implementation of the system on a PCB.

4. Control Software

4.1. General Information

To be able to test the hardware modules that are built around data converters, which are mixed-signal integrated circuits, it is necessary to develop software that could control them.

This software should run on the Raspberry PI 2 Model B (further RPi), which is a relatively weak single-PCB computer: it has 900 MHz SOC CPU, and 1 GB RAM. Therefore an interpreter or a virtual machine would take considerable amount of resources of this constrained environment. This fact suggests to use a *compiled* programming language like C for the development of the software. On the other hand, the modular structure of the battery testing system almost naturally implies an *object-oriented* language, with objects representing the hardware modules and components. The language that satisfies both criteria is *C++*.

Additional advantages of the C++ over C:

- Partition of the code into classes allows more clear structure of the code.
- Constructors and destructors help to automate initialisation and cleanup.
- Inheritance lets reusing of the code and has several more advantages, which will be discussed in Section 4.3
- The Standard Template Library (STL) containers and smart pointers render manual memory allocation unnecessary, thus preventing memory leaks.
- Much more convenient error handling with exceptions.
- Better type safety with `static_cast` and scoped enumerations.
- Templates permit to apply the same code to different data types.

Many features of the latest C++11 and C++14 standards were put to use.

As mentioned previously, RPi is a resource constrained system that complicates operation of an integrated development environment: already typing the source code

happens with a noticeable keyboard input lag. This makes source code development directly on the RPi quite inconvenient. That is why an alternative (and recommended [48]) method was used. That is, Netbeans 8.2 IDE, installed on a laptop directly connected [47] to the RPi, is used to develop the code, which is then remotely built on the RPi with g++ 4.9.2 (the latest version available for the RPi). This makes all the features of a modern IDE like debugging, automatic code completion, etc. available, while being run on a much faster MS Windows based machine.

A consistent coding style improves readability of the source code. In particular, the applied naming conventions is presented on Table 4.1.

Table 4.1.: Naming conventions used in the source code

Category	**Convention**	**Example**
variables	small letters, with words separated by underscore	`int new_variable`
functions	first word is small, additional words are capitalised and fused.	`getNewVariable()`
new types (`class`, `struct`, `enum`, `typedef`)	All words a capitalised and fused	`class NewClass`
macros and compile time constants	All capital letters, different words a separated with an underscore	`NEW_CONSTANT`

Exception are abbreviations, that capitalised. Additionally, some frameworks like Qt may have their own conventions. Then, those are used in the code that utilises the framework for consistency with it.

The software was first tested and used on the prototypes.

4.2. Design Goals

The software must control the components. In particular, this includes following main functionality:

- Configure components
- Set output voltage of the DAC
- Retrieve measured values

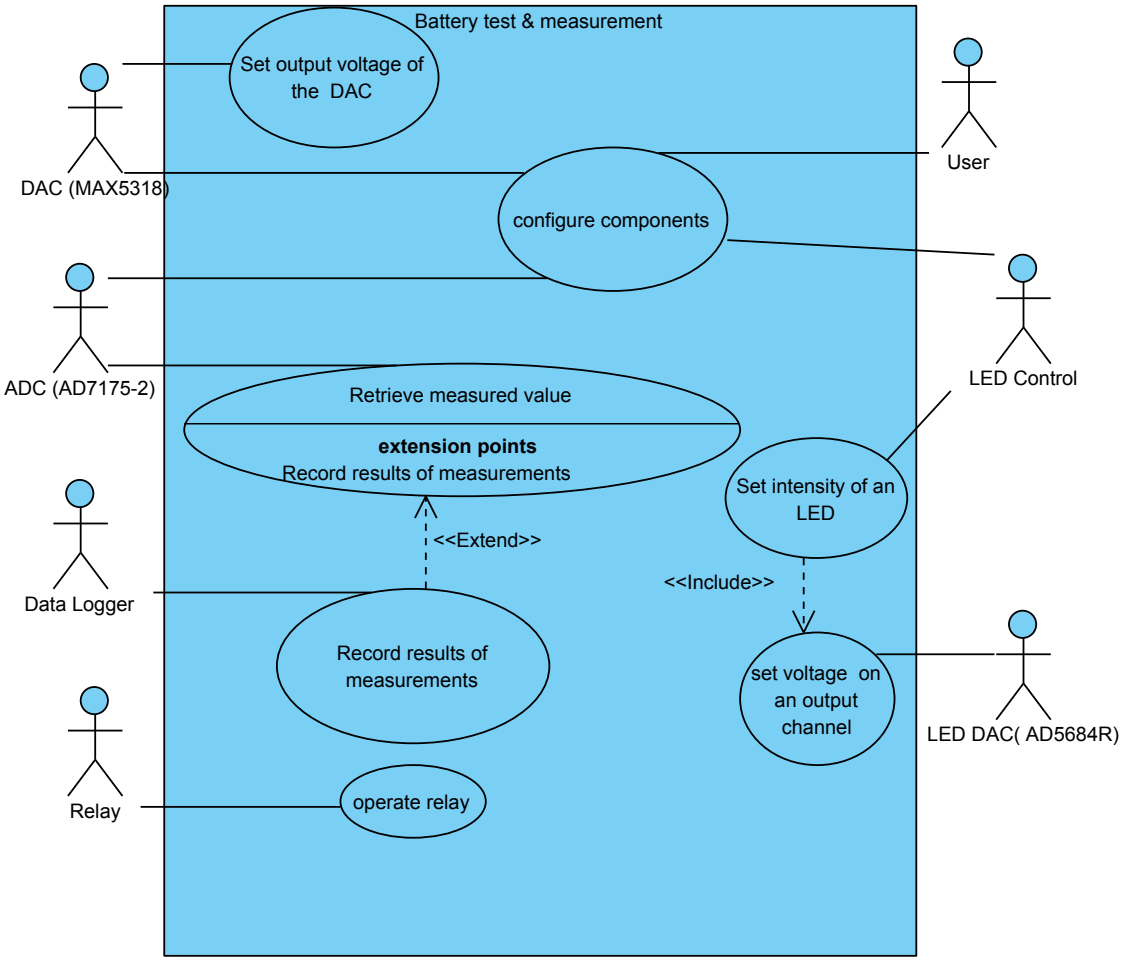

Figure 4.1.: Use case diagram of control software

- Record measurements
- Set LED intensity
- Operate the relay
- Other subordinate functions required to accomplish the tasks above

The functionality is illustrated by the use case diagram in Figure 4.1. It should be stressed that development of algorithms for constant current regulation is not a part of this thesis.

4.3. Architecture of the Battery Testing Library

This section offers a high level look on the software. Detailed description of all classes and functions is provided in Doxygen documentation on the DVD.

The design of the library is based on following principles:

Flexibility Make software externally configurable. Avoid hardcoding and magical numbers.

Reusability Allow the code to be shared if the objects have to perform same action. Avoid duplication of the code.

Extensibility Ability to extend the software with additional components, e. g. in case of hardware changes.

Convenience of use For developer it means automation of routine operations and simple interface. For user it means utilisation of GUIs.

Error checking Check every possible fault condition. Provide clear error messages.

In order to decouple the software from application it was designed as a library. This allows the code to be shared between applications. All members in the library are wrapped in `rpiio` namespace to prevent possible conflict with external code.

First of all the library needs some means to access GPIO pins and SPI interface. Therefore it was build on top of BCM2835 C library[1], which was put in a object-oriented wrapper. The first advantage of doing that is simpler interface. An example is shown in Table 4.2.

Table 4.2.: Comparison of bcm2835 library and Battery Testing Library. The user defines the pin once and no longer needs to pass the pin number, reducing probability of a bug.

BCM2835	Battery testing Library
`bcm2835_gpio_write(RPI_V2_GPIO_P1_05, LOW);`	`GPIOPin pin(5);` `pin.setState(State::LOW);`

Moreover, it allowed to add more functionality:

- The pin can be now referred by its number, instead of a hardcoded macro, which prerequisite of making them externally configurable.
- Automatic initialisation and closing of the bcm2835 library.

[1] http://www.airspayce.com/mikem/bcm2835/

- The library maintains a pin occupancy register and checks whether the pin is occupied prohibiting multiple assignment.

An example of configurability can be provided on basis of the `LEDControl` class. The class manages the LEDs and allows to set their intensity by percentage by adjusting output voltage of the AD5684R DAC. The assignment of LEDs to the outputs of the DAC is not fixed and can be configured. That means, it doesn't really matter to which output an LED is connected, because it can be set in software.

Inheritance is perhaps the most important tool in an object-oriented design. Firstly, it helps to avoid duplicating of common patterns. That way class `SPIDevice` provides SPI connection that is shared between all derived classes. It provides a `ChipSelect` object, avoiding separate duplicate declaration in every class that uses SPI. Moreover, the derived classes may benefit from its functions that let a value of any integer type to be sent over SPI, while also managing the chip select for the class.

Secondly, inheritance enables definition and enforcement of a unified interface by means of pure virtual functions, which turn classes into interfaces, because the derived classes are forced to override and implement them. For example class `DAC` has a pure virtual function`readCode()` , which will cause all `DAC` derived classes include this function resulting in consistent interface.

The base classes of data converters (`MeasurementDevice`, `ADC`, `DAC`) build a hierarchy of interfaces in such a way that an interface consists only of those functions that make sense for this particular category of devices. For example, function `enableChannel` makes sense only for data converters, but not for digital multimeters, therefore it is in the class `ADC`. All functions of `ADC` suit `DAC`, including `read()`, which would then be command to read back the output voltage. That is why `DAC` is derived from `ADC`.

This design opens possibility for a potential *polymorphic* implementation in the applications. That means that devices are declared by its category classes that may enable support for different hardware configurations without necessity to recompile.

Thirdly, reusing code and unified interfaces with inheritance facilitate extensibility. Deriving from a class equips the new class with some basic functionality, while interfaces make sure that it stays polymorphically consistent with devices in the same category.

Furthermore, inheritance allows to exploit similarity between devices for easy extensibility. For example AD5684R is a member of a family of 5 DACs that differ in

resolution and presence of internal reference. Once programming of one kind is accomplished it costed very little effort to add support for others, which was promptly done.

Error checking and handling is done with exceptions. They allow to propagate clear description of a fault condition in contrast to obscure return codes. In addition, they allow to handle errors, where it makes the most sense and free return values for more productive application. This already proved itself during testing by greatly simplifying identification for bugs. For more severe problems like potential null pointers debug assertions were used.

Finally, C++ templates is a very useful feature. Thanks to them, function `log` of class `DataLogger` supports arbitrary number of columns in row with any data type, for which stream insertion operator << is defined.

The class diagram of the library is depicted in Figure 4.2.

4.3.1. Concurrent Access to Digital Interface

The bcm2835 library operates directly with registers, which is fast but may cause conflict in case two applications try to use SPI concurrently. this was confirmed by a test depicted in Figure 4.3.

The first attempt to solve this problem is to add alternative implementation of SPI and GPIO pin control functions, that would use drivers (ioctl for SPI, sysfs for GPIO). This is slower, but the operating system would manage access to the interfaces. Unfortunately, this had only partial effect: the SPI transmissions were no longer mixed, but the chip selects still overlapped (Figure 4.4) .

The ultimate solution was to utilise system wide binary Linux semaphores in chip selects. The semaphore prevent activation of the chip select thus blocking SPI transmission until it becomes available. The disadvantage is that transmissions happen in bursts in each application. There is no way to synchronize them.

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4.3.2. Digital Interface Access over Drivers

Section 4.3.1 mentioned addition of an alternate method to access GPIO pins and SPI utilising facilities of the operating system. That are `sysfs` for the GPIO [50] and `spidev` driver [52] accessible with `ioctl` POSIX function [53].

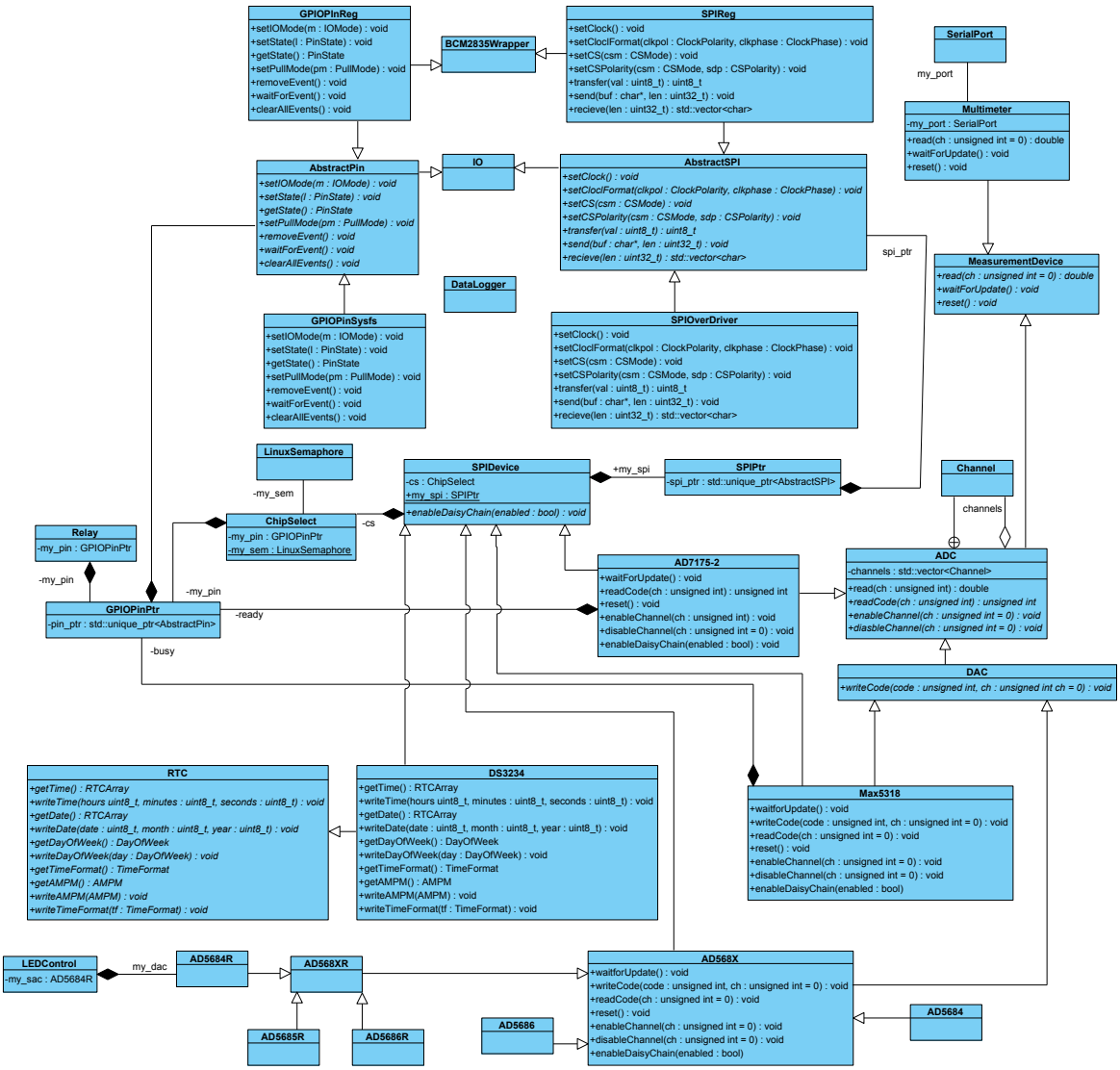

Figure 4.2.: Simplified class diagram of the battery testing library. Only members that establish associations or are part of interfaces are shown.

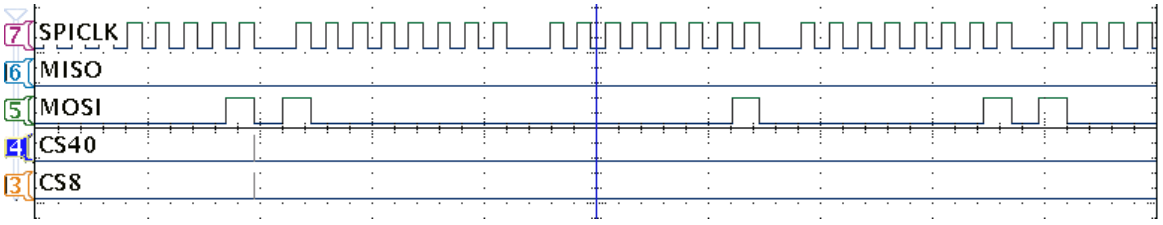

Figure 4.3.: Oscilloscope screenshot of 2 applications using SPI concurrently with register access The transmission is concurrent and mixed.

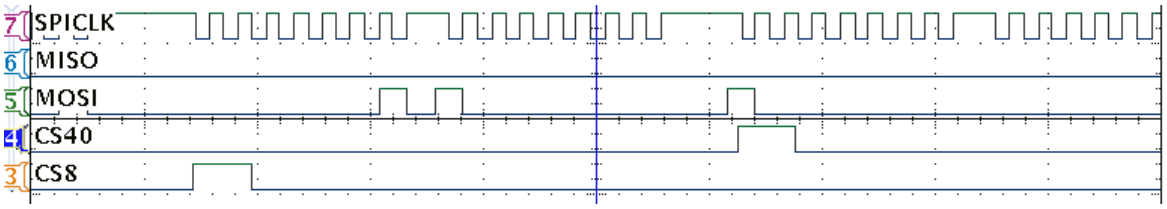

Figure 4.4.: Oscilloscope screenshot of 2 applications using SPI concurrently with access over OS The transmission is concurrent. Chip selects are overlapping.

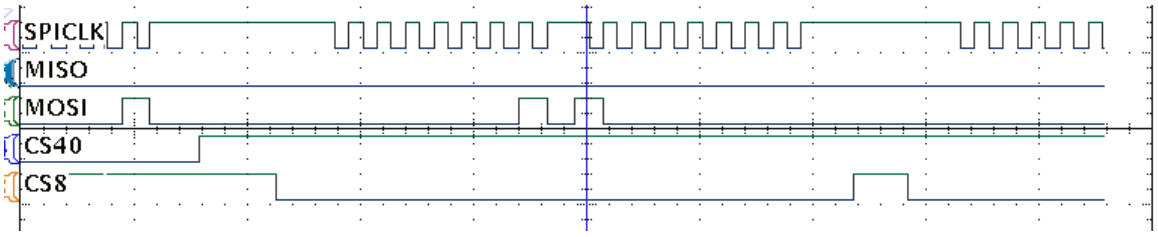

Figure 4.5.: Oscilloscope screenshot of 2 applications using SPI concurrently with semaphores The transmission is concurrent and now completely separated.

The library was then partially redesigned to give the user option to choose a particular access option. This can be done in multiple way, summarised in Table 4.3. First, the user could pick a suitable class that implements it. But perhaps better way would be to use typedefs, which resolves in driver implementation if `OS_IMPL` is defined and in register implementation otherwise. Thus, it would be possible to change the implementation by macro un/definition and recompiling.

Finally, there are smart pointer like classes that use polymorphic approach to defer the choice until run-time. It is done by `setImpl` function, which sets a global variable. Default is access over registers. This method is used throughout the library to offer access option choice without recompiling the library. Thus, the user has freedom to decide, whether components would communicate using SPI over registers or SPI over drivers.

Table 4.3.: The methods to choose digital interface implementation.

Choice method	**GPIO pin**	**SPI**
Fixed to register implementation	class `GPIOPinReg`	class `SPIReg`
Fixed to driver implementation	class `GPIOPinSysfs`	class `SPIOverDriver`
Macro `OS_IMPL`	typedef `GPIOPin`	typedef `SPI`
Polymorphic	class `GPIOPtr`	class `SPIPtr`

4.4. LED Control Manager Application

At the request of a BATSEN member an application was developed that is capable of:

- Managing assignments of colour channels to DAC outputs
- Reading channel setting as well chip sellect pin number from a configuration file.
- Managing a list of LED intensities with duration of their application and stepping through this list.
- Saving this list to a configuration file and reading from it.

To simplify the usage, a GUI was made in Qt (a GUI framework). (Figure 4.6).

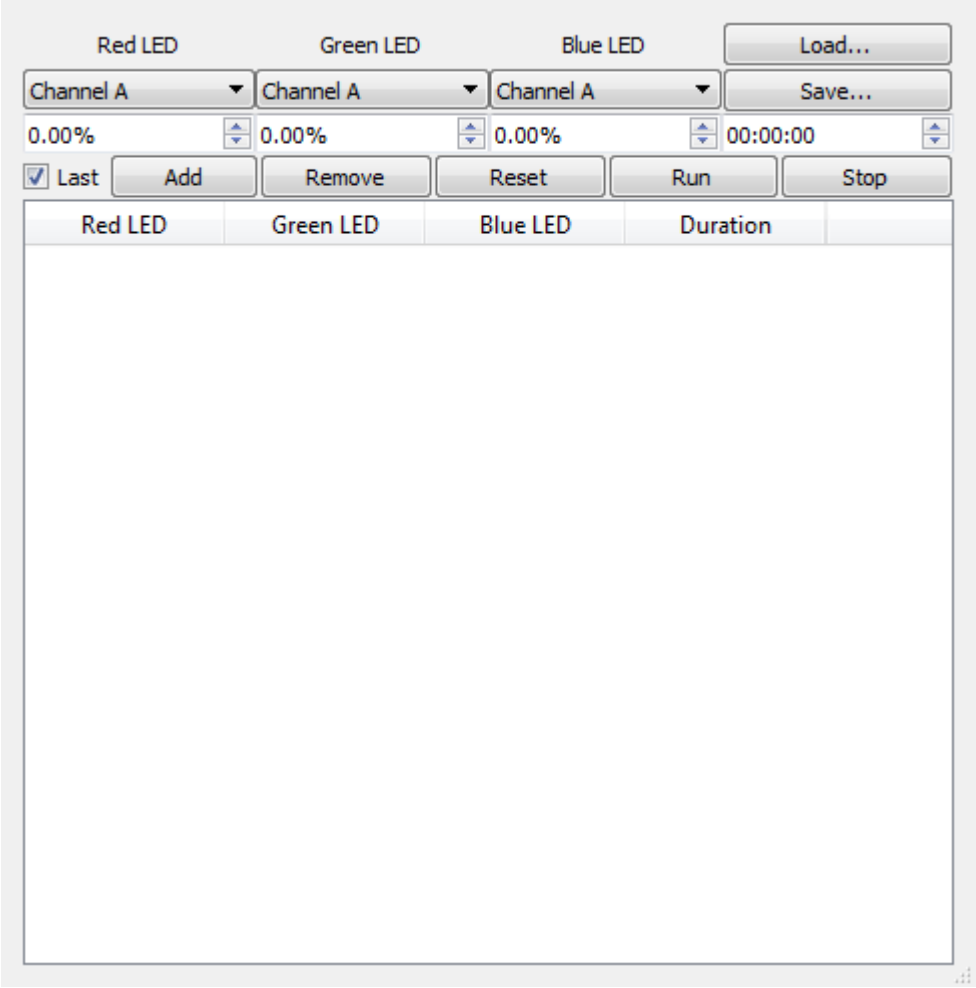

Figure 4.6.: The GUI of LED Control Manager

5. Implementation on the Printed Circuit Board

5.1. PCB Design

The PCB design of the battery measurement system was done in Eagle CAD. It followed the procedure:

1. Prepare full schematic. Add components and make symbols and footprints as necessary.
2. Define dimensions and the positions of the mounting holes of the PCB.
3. Set at least rough placement of connectors.
4. Perform principal placement of components. Then place and root belonging passive components.
5. Route critical circuits for function first. That are circuits involved in measurement and charging/discharging.
6. Route power supply circuitry.
7. Route digital connections.
8. External review of the design and a review by manufacturer.

5.1.1. Schematic

The schematic was first drawn, like stated in the list above. The footprints for the integrated circuits were obtained from vendors in Ultra Librarian format. The Ultra Librarian software then was used to import them to Eagle. In addition the footprints of 0306 capacitors and 0805 3-terminal capacitors had to be designed according their data sheets.

The schematic is shown in Figure 5.1. A few commentaries are perhaps necessary.

- The R1 resistor serves safely discharging the capacitors on the board and external PS after cutting off the power.
- The 3.3 V on Raspberry Pi is produced by a switching buck converter. C7 attempts to block the switching noise from it.
- The resistors R4-R15 implement the resistor network described in Section 3.9.1. The 0 Ω resistors serve like jumpers, which are either occupied or soldered together as necessary to get required resistant and current. The Table 5.1 lists needed connections to get a desired current option.

Table 5.1.: List of connections necessary to get a current range

Max. current	Jumpers that must be shorted
1 mA	R8
3.33 mA	R11,R10,R13
5 mA	R11, R10, R12
10 mA	R15
15 mA	R11, R10, R12, R15
20 mA	R9, R11, R14
30 mA	R15, R14, R9, R11

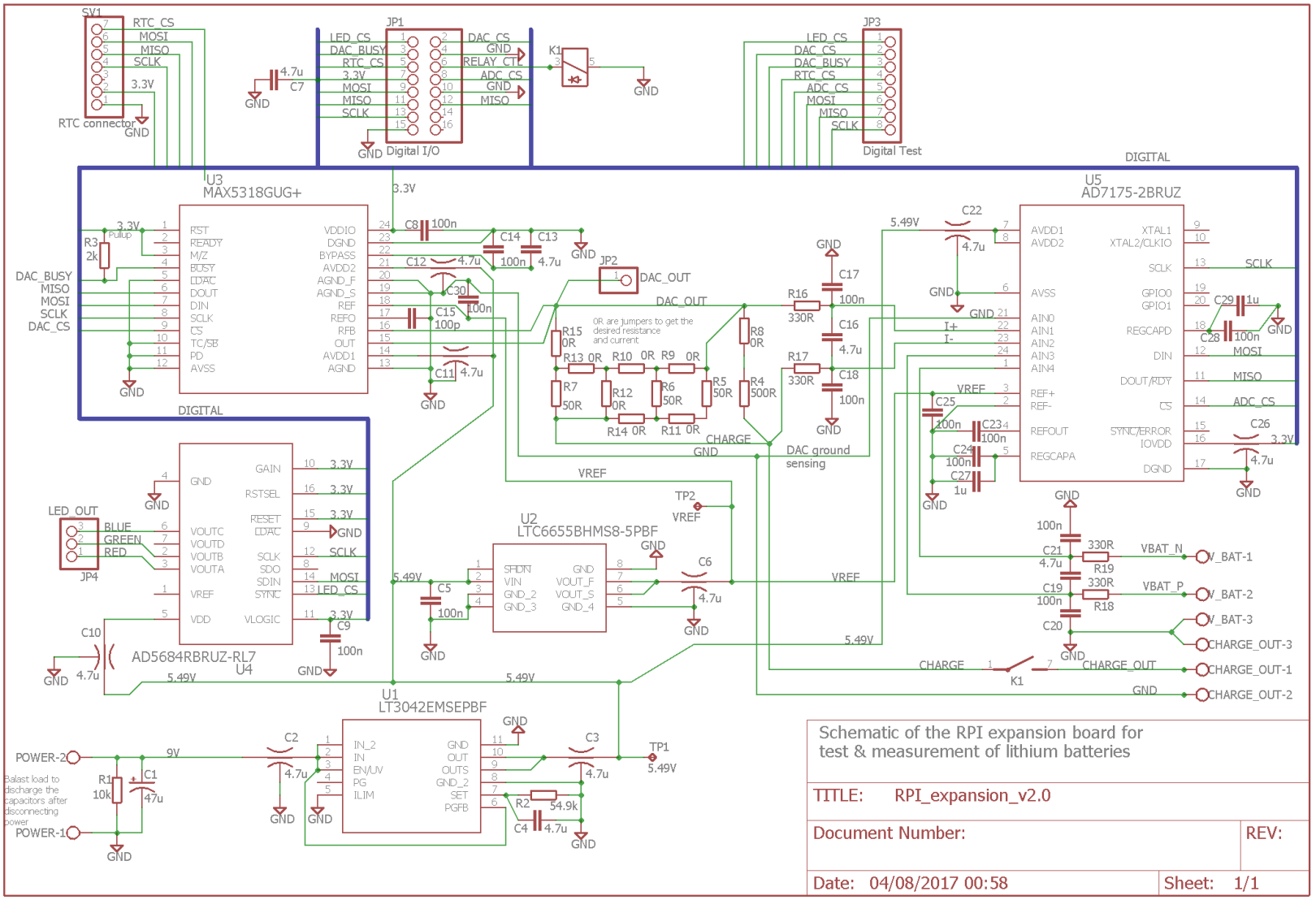

Figure 5.1.: Schematic of the battery measurement board

5.1.2. Layout

The first step is to define dimensions and position of mounting holes. The simpler design permits smaller size then the predecessor. The board was designed as HAT (hardware attached on top), that is to be placed directly above Raspberry Pi and connected to it over a downward female pin connector. Only a range Raspberry Pi pins were occupied. This required precise placement of the connector and mounting holes.

The board was given a *solid* ground plane in the form of a copper pour on the bottom side. Splitting ground plane into analog and digital parts is sometimes preferred with data converters placed between them. Nevertheless, this is neither necessary [41] nor possible, because MAX5318's and AD7175-2's packages don't have clear separation into analog and digital parts. Anyway, despite the data converters have DGND and AGND pins, both of them must be connected to analog ground plane [43].

This configuration, however, demands careful placement of the components under consideration of *return currents* in the ground plane. Care should be taken that digital and analog return currents do not cross [43]. That is why imaginary analog and digital areas were defined notwithstanding the solid ground plane. The boundary lies roughly on the 5.49 power supply track. Accordingly, the data converters were manually placed in a way that their predominantly digital ends face towards the digital connector on top.

The traces between the pins and bypass capacitors must be short in order to effective [43]. The layout goes into great lengths to put them as close to the pins as possible.

The ground plane must be unbroken to be effective [43]. Therefore the effort was made to manually route as much as possible on top with only short flyovers on the bottom. Additionally, return currents were taking in account. For example, the vertical flyovers were preferred in the digital area of the PCB in order not to obstruct return currents flowing towards digital ground pins.

Also an attempt was made to follow the layout recommendations of the manufacturers in data sheets as well as possible. That is the reason for following oddities of the layout (Figure 5.2):

- The return current does not go directly to ground, because a star ground connection described in [44, p. 22, 23, 37] was implemented.
- The polygon on the top layer near LT3042 LDO is the guard ring recommended by [45, p. 12-13].

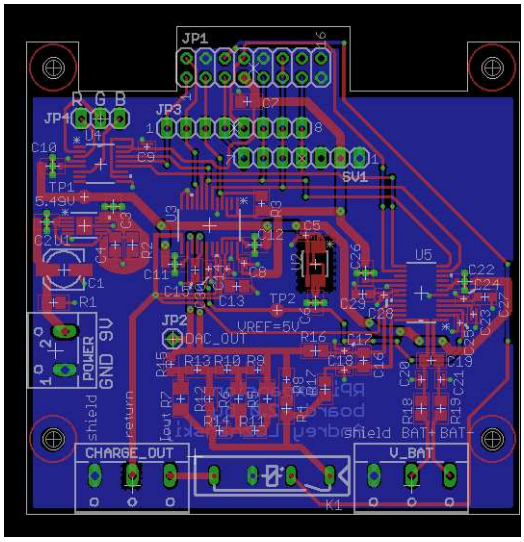

Figure 5.2.: The layout of the measurement board

- [46, p. 14] discourages ground plane under LT6655, therefore it is cut out.

5.2. Assembly and Testing

The manufactured board was assembled manually module by module mainly using solder paste and hot air. That allowed to test each module. The voltage regulator and reference with the belonging passive components were installed first because other components depend on them. Electrical connections and absence of shorts were also continually verified.

The board was assembled and tested in following order.

1. Voltage regulator. Output voltage of 5.47 V was slightly below design, but still acceptable.
2. Voltage reference. 5 V output was confirmed
3. 5684R DAC. The correct default output voltage of 2.5 V gave strong clue the it functions normally.
4. MAX5318 DAC. The correct default output voltage of 2.5 V gave strong clue the it functions normally.

5. AD7175-2 ADC. The output of the internal reference of 2.5 V gives only small hint about correct work. The only way to make sure it is operable is actually to read a value.
6. The rest of components: shunt resistors, connectors, relay. Special attention was given to the latter, because incorrect installation of it can damage Raspberry Pi.

The assembled PCB is shown in Figure 5.3. It could be attached to Raspberry PI as HAT like it was designed.

5.2.1. ADC (AD7175-2)

The results of the final tests are summed up in Table 5.2

Table 5.2.: Summary of the tests results of the measurement module. qtStrongest current means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Function	**Parameter**	**Design Target**	**Achieved**	**Proof**
Voltmeter	Lowest voltage at battery	1 V	0 V	Ensured by design
	Highest voltage at battery	5 V	5 V	Ensured by design
	Accuracy	1 mV	70 μV?	Figure B.31, Figure B.30. Hard to test due to low precision of digital multimeters.
	Precision	1 mV	300 nV	Ensured by the LSB of the ADC
	Largest noise	50 $\mu V_{p\text{-}p}$	$\sim$4.5 $\mu V_{p\text{-}p}$, 5 $\mu V_{p\text{-}p}$ real world with shielding	Figure B.34, Figure B.41
Ammeter	Weakest current	±1 μA	±1 μA	Ensured by design

Table 5.2.: Summary of the tests results of the measurement module. qtStrongest current means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Function	Parameter	Design Target	Achieved	Proof
	Strongest possible current	±1 mA	±30 mA	Ensured by design. See also Section 3.9.1
	Worst accuracy	0.1‰ of strongest current	50 ppm after self-calibration	Figure B.48, Figure B.47
	Worst precision	0.1‰ of strongest current	1.2 ppm with external reference, 0.6 ppm with internal reference	Guaranteed by LSB and shunt resistance of the ADC. Equation 3.14
	Largest noise	0.1‰ of strongest current	5 ppm, 4-8 ppm real world with shielded cable	Figure B.42, Figure B.43
	Sampling rate	50 SPS	100 SPS, 50 SPS for Voltmeter and Ammeter	Supported by the ADC

The measurement module built around AD7175-2 fulfilled the specification requirements. The PCB implementation demonstrates improvement in noise performance compared to demo board.

5.2.2. DAC (MAX5318)

The results of the final tests are summed up in Table 5.3

Table 5.3.: Summary of the final tests results of the current regulator module. qtStrongest current means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Parameter	Design Target	Achieved	Proof
Smallest current	±1 μA	±1 μA	Ensured by the design

Table 5.3.: Summary of the final tests results of the current regulator module. qt-Strongest current means upper bound of current at tested shunt resistance (500 Ω) and is *1 mA*.

Parameter	**Design Target**	**Achieved**	**Proof**
Strongest current	$\geqslant$±1mA	±30 mA	Table B.2, Table B.2, Figure B.13
Worst accuracy for current	0.1‰ of strongest current	Could not be not tested due to lack of constant current regulatioon	
Worst precision for current	0.1‰ of strongest current	$\sim$38 ppm.	Ensured by the LSB of the DAC and shunt resistance
Lowest battery voltage	1 V	1 V- 0.5 V depending on discharging current	ensured by design
Highest battery voltage	4.5 V	4.5 V	Ensured by design
Precision of battery voltage	50 μV	$\sim$20 μV	Ensured by LSB of the DAC
Accuracy of battery voltage	50 μV	2.06 LSB after calibration $\approx$40 μV	Figure B.14, Figure B.15

The current regulator module built on basis of MAX5318 fulfilled all measurable specifcation requirements.

5.2.3. DAC for LED Control (AD5684R)

Since no variable parameters are defined for LED control module Table 3.3 remains valid. The thing is to ensure that the DAC is working properly: the DAC is responsive to the instructions from Raspberry Pi and all channels set the commanded voltages. This was done without an issue.

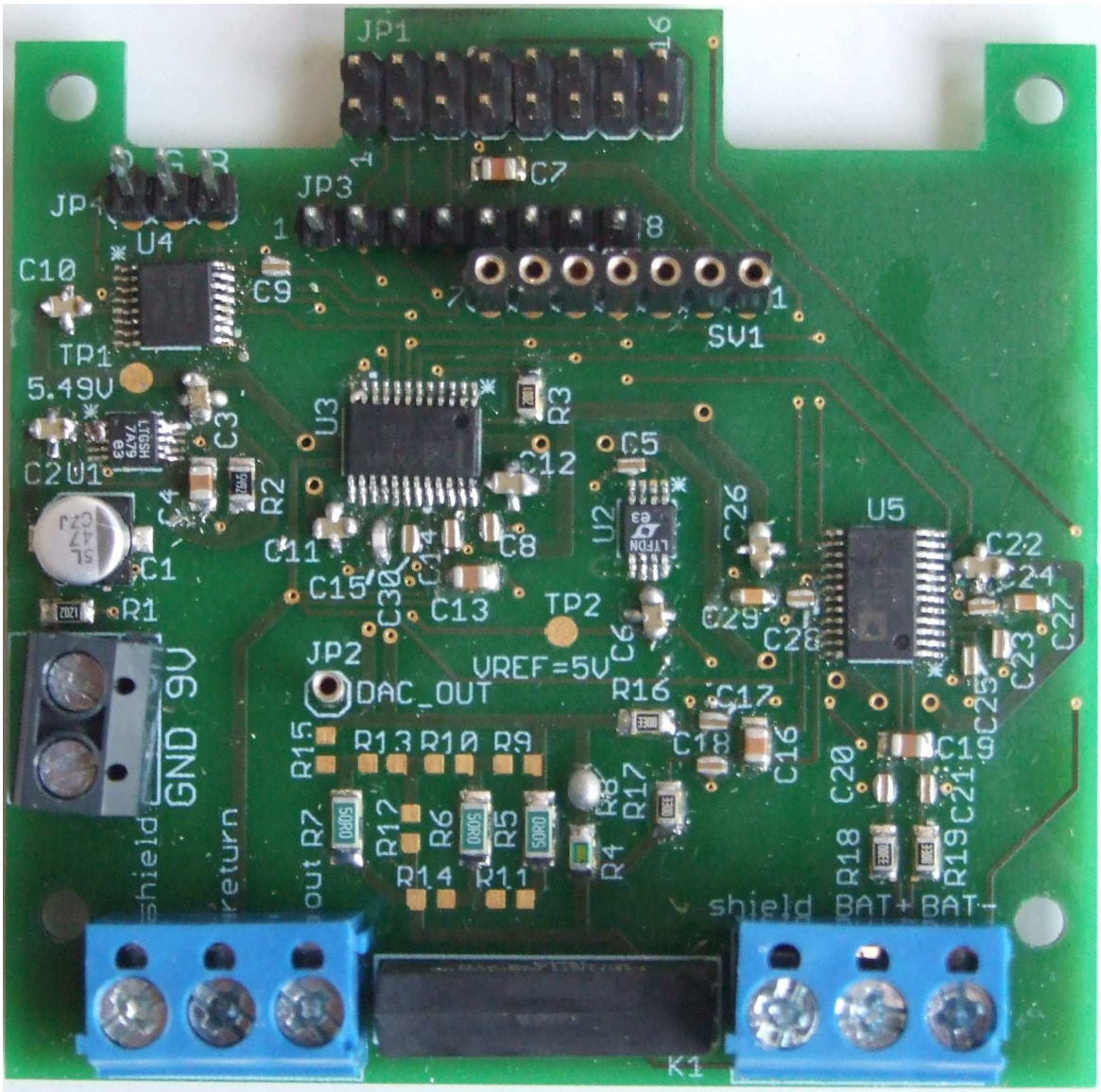

Figure 5.3.: The assembled PCB of the battery testing system. The downward female pin connectors were replaced with upward male ones.

6. Summary and Outlook

This chapter sums up the thesis and compares the accomplished results with the specification. The outlook provides suggestions for further developments.

6.1. Summary

The task was to develop a Raspberry Pi expansion board capable of precise measuring and setting the voltage and current. In addition, it should be able to control 3 external LEDs.

First the previous implementation was analysed for problems. Then the goals of the new implantation and a clear specification were defined. After consideration of alternative concepts different implementation options were looked into and suitable components were selected. A close attention was paid to noise and countermeasures to it. Then the hardware submodules were prototyped and tested. Finally, the system was implemented on a PCB and tested.

Nothing of that, however, could be possible without supporting software. The software extensive is library that handles everything from basic functions of Raspberry Pi, like GPIO pins and SPI interface to controlling of the components of the board.

6.2. Evaluation

The project ended in a great success, subject to unnoticed errors. The targets for measurement accuracy were met, while minimum targets for precision and noise were exceeded by an order of magnitude. Thus, the board is capable of precise, high resolution measurements. The current regulation module was also on specification with the bonus of current capability of up to ±30 mA.

The only cloud on a clear sky is that there was some hints about long settling time after a large step (example Figure B.35). This wasn't investigated.

LED Control works fine, but lacks calibration for non linear behaviour of the LEDs.

The software turned out to be flexible, easy to use,reusable, extensible and with convenient error handling procedures.

6.3. Outlook

Like already mentioned, the large step in measured quantities might result in a long settling time. Therefore, this case should be investigated if such a problem exists and, if necessary, corrected. In addition the operation at currents >1 mA has to be tested.

The board by itself is unable to regulate current. So software for current regulation has to be adapted to be used with the board. However, the hardware methods should not be dismissed, because only they are capable to achieve truly constant current.

The board is supposed to work in conjunction with a camera performing optical observation, so synchronisation must be achieved. Such observation may involve lighting with LEDs. The LEDs have to be calibrated. That is, the dependence of luminosity on control voltage has to be examined.

Finally, the measurement of temperature has to be implemented as a standalone module.

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Appendix A.

Lists of Candidate Parts

Table A.1.: Candidate DACs

Manufacturer	**Model**	**Resolution**	**Accuracy (typ./ max.),** LSB	**Samples available?**	**Price on Mouser**	**Broadband noise,** $\mathrm{nV}/\sqrt{\mathrm{Hz}}$	**Pro**	**Contra**
Maxim Integrated	MAX5318	18	0.5/2	yes	€22,5	26	High current capability, possibly without external buffer?	VDD-0.1 V_{ref} range
Analog Devices	AD5780	18	1 LSBs max	yes	€42,3	8	High accuracy, wider output range possible <0 V >5 V, very low noise	Complicated: requires negative supply. Expensive to buy

Table A.1.: Candidate DACs

Manufacturer	**Model**	**Resolution**	**Accuracy (typ./ max.),** LSB	**Samples available?**	**Price on Mouser**	**Broadband noise**, $\mathrm{nV}/\sqrt{\mathrm{Hz}}$	**Pro**	**Contra**
Analog Devices	AD5790	20	2 LSBs max	yes	€93,35	8	Same as AD5780	Same as AD5791. Very expensive to buy
Texas Instruments	DAC9881	20	2/3 or 1/2	no	€28,91/ €38.48	30	Kelvin senses for ref voltage input	Not easily available
Texas Instruments	DAC1220	20	15 ppm	no	€14,92	600 at 100 Hz	Delta-Sigma, cheapest	Lower accuracy, very high noise

Table A.2.: Candidate buffer operational amplifiers. The low frequency noise was calculated with the tool by Intersil [15].

Vendor	**Model**	**Broadband noise floor,** $\mathrm{nV}/\sqrt{\mathrm{Hz}}$	**Est. 1/f corner frequency,** Hz	**Calc. noise 0.1 to 100 Hz,** μV_{rms}	**Max. power supply span,** V	**Rail-to-Rail**	**Simulated voltage swing (mV) to positive, negative rail at current points:**			**Samples available?**	**Price on Mouser**	**Pro**	**Contra**
							±1 mA	**±30 mA**	**±50 mA**				
Analog Devices	AD8615	10	400	0.54	5	IO	-16.7, 7.8	-301.5, 247.37	-527.5, 434.24	yes	€1.91	Higher current, low 20 MHz BW	Higher noise
Analog Devices	AD8655	4	1030	0.34	5	IO	-19, 11.8	-317.3, 368	-539.75, 635.1	yes	€ 1.94	Less noise, low 28 MHz bandwidth	
Analog Devices	ADA4895	1	8	0.01	10	O	-797.8, 71.14	-797.8, 199.657	-840, 687	yes	€4.31	Very low noise, wider supply range	>10 Gain stable? Large voltage swing
Analog Devices	ADA4897	1	8	0.01	10	O	-70.55, 70.56	-73.11, 70.66	-102.62, 81.54	yes	€4.49	Very low noise, wider supply range, high voltage swing, disable	voltage swing at low current, input bias current
Texas Instruments	LMP7701	9	13	0.12	12	V-, O	-23.3, 23.2	-726.2, 726.3	-962.45, 962.5	no	2.37/2.56		large swing
Texas Instruments	OPA209	2.25	20	0.04	36	O	-1.5/1.5 V	-1.5/1.5 V	-1.5/1.5 V	no	2.64	very low noise, wide supply range, 18 MHz BW	not rail-to-rail in, -1.5 V common mode voltage limitation

Table A.3.: Candidate SPST reed relays

Vendor	**Model**	**Nominal coil voltage, V**	**Coil resistance, Ω**	**Surface dimensions, L×W, mm**	**Price**	**Advantage**
Hamelin	HE721A0510	5	500	20×7.5	1.98	Built in flyback diode
Hamelin	HE3621A0510	5	500	19×5	1.98	Built in flyback diode
Meder Standex	SIL03-1A72-71D	3	500	19.8×5.08	3.64	May be controlled directly from RPi, 0.5 ms operating time, flyback diode
Hamelin	HE3321A0500	5	500	24×7	N/A	Model previously in use
Coto Technology	9001-05-01	5	500	19.8×5.08	3.93	Flyback diode, 0.35 ms oprating time
Coto Technology	9007-05-01	5	500	19.8×5.08	1.57	Flyback diode, 0.5 ms operating time
Coto Technology	8L01-05-011	5	500	19.8×5.08	2.87	Flyback diode, 0.5 ms oprating time

Table A.4.: Candidate ADCs for standalone ammeter

Vendor	**Model**	**Linearity**	**Max. supply voltage, V**	**Absolute input range with buffers, V**	**Absolute voltage range without buffers, V**	**Differential input range, V**	**Noise in V_{rms} at sample rate**	**Max. sample rate**	**Sample available?**	**Price on Mouser**	**Pro**	**Contra**
Texas Instruments	ADS1259	10 ppm	5.25	absent	V_{ss} to V_{dd}	$\pm V_{ref}$	4/60	14.4 kSPS	No	13.50	Internal reference, calibration, integrity check	no buffers
Texas Instruments	ADS1225	20ppm	5.5	0.1 to V_{dd}-1.5 V	V_{ss} to V_{dd}	$\pm V_{ref}$	15/100	16 or 100 SPS	No	5.93	simple operation, internal self-calibration.	buffer unusable, high noise
Texas Instruments	ADS1255	10ppm	5.25	0.1 to V_{dd}-25 V	V_{ss} to V_{dd}	$\pm 2V_{ref}$	0.815/100	30 kSPS	No	11	low-noise, high effective resolution, PGA .	buffer unusable
Analog Devices	AD7791	15ppm	5.25	0.1 to V_{dd}-0.1 V	V_{ss} to V_{dd}	$\pm V_{ref}$	high	120 SPS	No	5.93	somple operation, internal self-calibration.	buffer unusable, high noise

Table A.4.: Candidate ADCs for standalone ammeter

Vendor	**Model**	**Linear-ity**	**Max. supply voltage, V**	**Abso-lute input range with buffers, V**	**Abso-lute voltage range without buffers, V**	**Differen-tial input range, V**	**Noise in V_{rms} at sample rate**	**Max. sample rate**	**Sample avail-able?**	**Price on Mouser**	**Pro**	**Contra**
Linear Techno-logy	LTC2440	15ppm	5.5	absent	0.1 to V_{dd}	$\pm V_{ref}/2$	0.75/110	4 kSPS	yes	6.5	continual self-calibration, low noise	no buffer

Table A.5.: Candidate ADCs for the voltmeter.

Vendor	**Model**	**INL**	**Absolute inpute range, V**	**V_{ref} range, V**	**Max. sample rate**	**Sample available?**	**Price on Mouser**	**Remarks**
Maxim Integrated	MAX11154	6 LSB	0 to V_{ref}	0 to 5.1	500 kSPS	yes	n/a	
Linear Technology	LTC2364-18	2 LSB	0 to V_{ref}	0 to 5	250 kSPS	yes	5.7	more accurate

Table A.6.: Candidate multichannel ADCs for combined voltmeter/ammeter

Vendor	**Model**	**Resolution**	**Channel configuration**	**Linearity**	**Max. supply voltage range**	**Absolute input range with buffers, V**	**Absolute input range without buffers, V**	**Differential input range, V**	**Noise at sample rate, V_{rms}**	**Max. sample rate**	**Samples available?**	**Price on Mouser**	**Pro**	**Contra**
Analog Devices	AD7172-2	24	2 diff./ 4 pseudo	5 ppm	5.5	GND to AVdd	GND to AVdd	$\pm V_{ref}$	0.62 at 60 SPS	31250 SPS	yes	12	very low noise, extremely flexible input config, self calibration	somewhat complicated programming
Analog Devices	AD7175-2	24	2 diff./ 4 pseudo	7.8 ppm	5.5	GND to AVdd	GND to AVdd	$\pm V_{ref}$	0.23 at 60 SPS	250 kSPS	yes	19.5	ultra low noise, higher eff. res., extremely flexible input config, self calibrtion	somewhat complicated programming
Analog Devices	AD7177-2	32	2 diff./ 4 pseudo	7.8 ppm	5.5	GND to AVdd	GND to AVdd	$\pm V_{ref}$	0.13 at 60 SPS	10 kSPS	yes	24	extreme low noise, higher eff. res., extremely flexible input config, higher self calib	somewhat complicated programming

Table A.6.: Candidate multichannel ADCs for combined voltmeter/ammeter

Vendor	**Model**	**Resolution**	**Channel configuration**	**Linearity**	**Max. supply voltage range**	**Absolute input range with buffers, V**	**Absolute input range without buffers, V**	**Differential input range, V**	**Noise at sample rate, V_{rms}**	**Max. sample rate**	**Samples available?**	**Price on Mouser**	**Pro**	**Contra**
Analog Devices	AD7799	24	3 diff.	15	5.25	±100 mV from rails	GND to AVdd	$\pm V_{ref}$	2.95 at 60 SPS	470	5 pieces at hand	9.1	PGA	Significantly worse characteristics, reduced input range with buffers

Table A.7.: Candidate LDO voltage regulators

Vendor	Model	**Accuracy, %**	**Wideband noise**, nV/rtHz	Noise 10 Hz to 100 kHz, μV_{rms}	**Vin max, V**	**Output current, mA**	**Samples available?**	**Price on Mouser**	**Advantages**
Analog devices	Ad7118	1.8% max.	30	11	20	200	yes	1.96	Low noise, thermal protection
Linear Technology	LT3042	2 mV	2	0.8	20	200	yes	4.41	high accuracy, multiple protection, very low noise.

Table A.8.: Candidate Voltage references

Vendor	**Model**	**Accur-acy, %**	**Temco, ppm/°C**	**Wide-banad Noise, nV/rtHz**	**Noise 0.1 to 10 Hz, μV_{p-p}**	**V_{in} max, V**	**Dropout Voltage at 0 mA / 2 mA load, mV**	**Samples available**	**Price on Mouser**	**Pro**	**Contra**
Analog Devices	ADR4550	0.02/0.04	2/4	95	2.8	15	100/200	Only A GRade	5.5/7.00		
Intrersil	ISL2190	0.25	7	100	4.2	36	unknown	yes	6		
Maxim Integrated	MAX6126A	0.02/0.04	3/5	95	2.85	12.6	<100	yes	3.63/5.25	Kelvin sense, low dropout	
Maxim Integrated	MAX6350	0.02	1/1.5/2.5	21	3	36	3000	yes	9.16/10.82	lowest tempco, low wideband noise, trim	large dropout
Maxim Integrated	MAX6250A	0.02	2-8	21	3	36	3000	yes	3.81-7.2	low tempco, low wideband noise, trim	large dropout
Maxim Integrated	MAX6070	0.04	6	100	9	5.5	150 max.	3.03	no	compact SOT package	higher noise
Maxim Integrated	MAX6143A	0.06	3		9	40	2	yes	5.69		
Maxim Integrated	MAX6175A	0.05	3		9	40	2	no	4.62		

Table A.8.: Candidate Voltage references

Vendor	**Model**	**Accur-acy, %**	**Temco, ppm/°C**	**Wide-banad Noise, nV/rtHz**	**Noise 0.1 to 10 Hz, μV_{p-p}**	**V_{in} max, V**	**Dropout Voltage at 0 mA / 2 mA load, mV**	**Samples available**	**Price on Mouser**	**Pro**	**Contra**
Linear Techno-logy	LT6655B	0.025	2	84	1.25	13.2	200-500 max.	yes	11	High accuracy, very low noise, low tempco	
Linear Techno-logy	LT6652A	0.05	5		2.8	13.2	300	yes	6.09		
Linear Techno-logy	LT1027B	0.05	2	20	3	40		3000	yes	8.37	
Linear Techno-logy	LT6654A	0.05	10		2.2	36	100-450 max	yes	5.85		
Linear Techno-logy	LT1236A	0.05	5		3	40	2200	yes	9.27		

Appendix B.

Test Procedures and Results

B.1. Noise and Countermeasures

B.1.1. Simulation of Bypass Capacitors

The frequency response of the bypass capacitors was simulated in Matlab where a capacitor is modelled as capacitance in series with its parasitics. The complex impdance

$$\bar{Z} = \frac{1}{j2\pi fC} + ESR + j2\pi f \cdot ESL$$

is computed at frequencies from 10 Hz to 5 GHz and plotted. The pairs of capacitors are calculated in parallel combination.

$$\bar{Z} = \frac{\bar{Z}_1 \bar{Z}_2}{\bar{Z}_1 + \bar{Z}_2}$$

The real-world values for ESR and ESL are taken from Murata's SimSurfing tool[1].

[1] http://ds.murata.co.jp/software/simsurfing/en-us/index.html

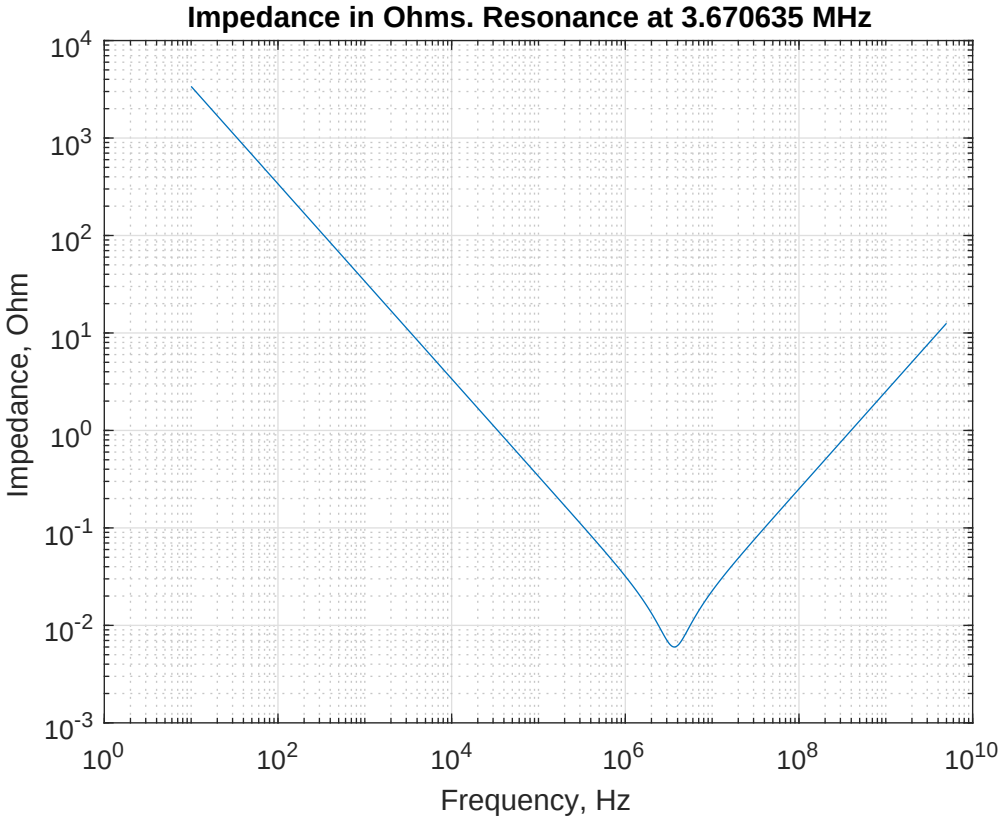

Figure B.1.: Simulation of the frequency response of a capacitor. The capacitor is Murata GRM21BR71E475KA73 (4.7 μF, 0805) with ESR=6 mΩ and ESL=400 pH.

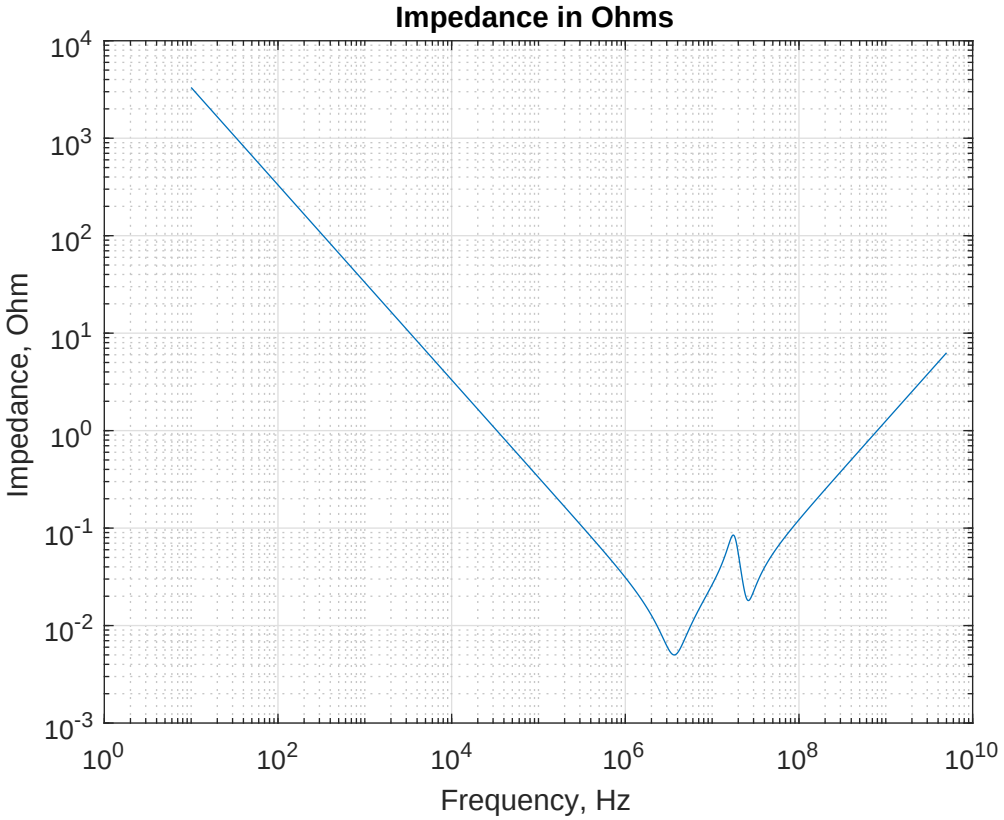

Figure B.2.: Simulation of a parallel combination of bypass capacitors. The capacitor are:
Murata GRM21BR71E475KA73 (4.7 μF, 0805) with ESR=6 mΩ and ESL=400 pH,
Murata GRM188R71E104KA01 (100 nF, 0603) with ESR=20 mΩ and ESL=400 pH.

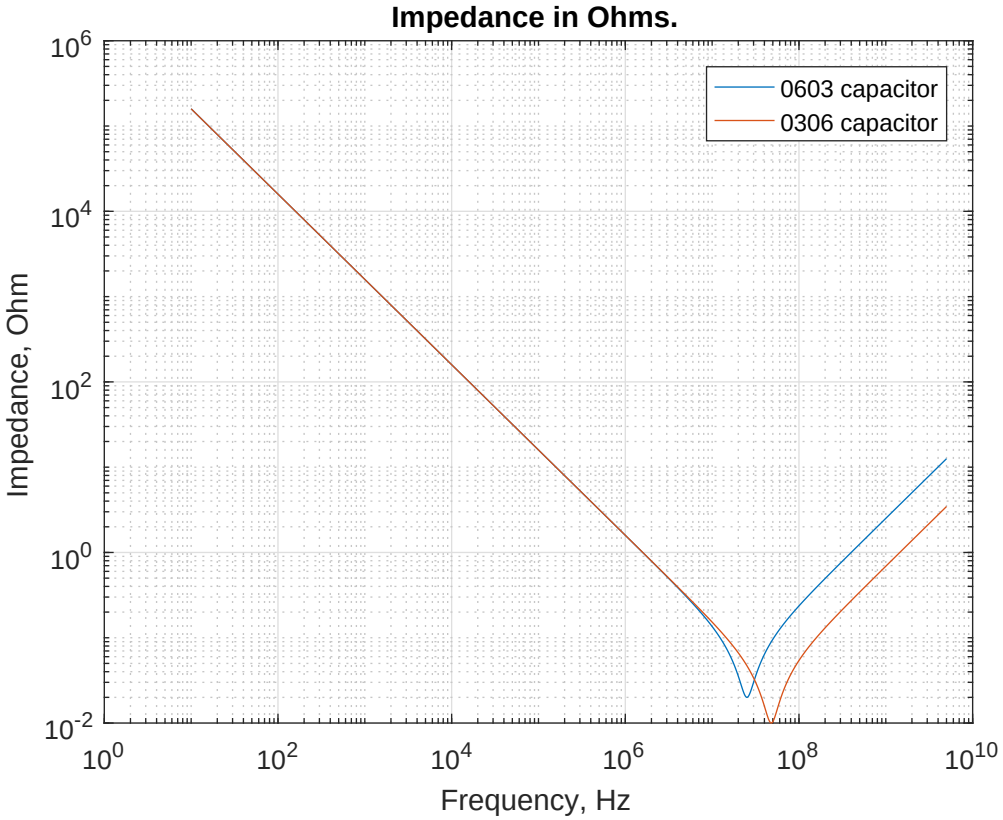

Figure B.3.: Comparision of impedance responses of 0603 and 0306 capacitors The capacitors are:
Murata GRM188R71E104KA01 (100 nF, 0603) with ESR=20 mΩ and ESL=400 pH
Murata LLL185RZ1A104MA01 (100 nF, 0306) with ESR=10 mΩ and ESL=110 pH

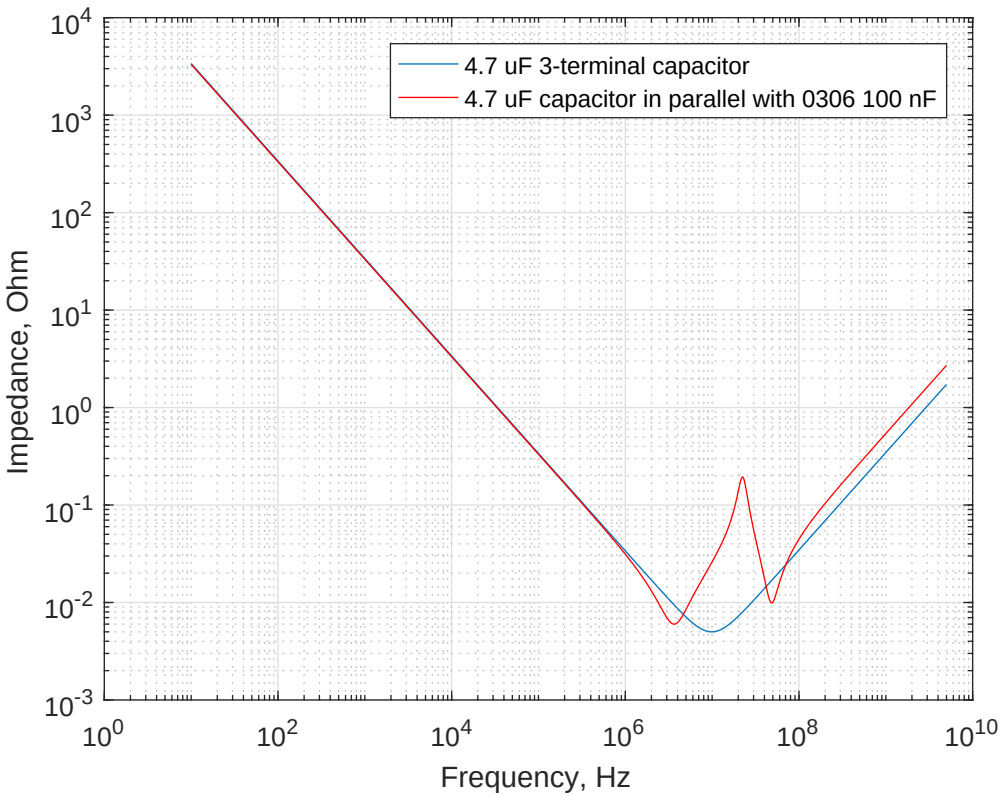

Figure B.4.: Comparision of a 3-termainal capacitor with a combination of 2 capacitors. The 3-terminal capacitor is Murata NFM21PC475B1A3 (4.7 μH, 0805) with ESR=5 mΩ and ESL=55 pH
The two other capacitors are:
Murata GRM21BR71E475KA73 (4.7 μF, 0805) with ESR=6 mΩ and ESL=400 pH,
Murata GRM188R71E104KA01 (100 nF, 0603) with ESR=20 mΩ and ESL=400 pH,
Murata LLL185RZ1A104MA01 (100 nF, 0306) with ESR=10 mΩ and ESL=110 pH.

B.1.2. Measurement of Common Mode Noise

In order to determine, what kind of common mode noise is to be present in the measurement environment, an 1.8 m unconnected cable was probed with an oscilloscope. Figure B.5 presents the full signal. The signal is band limited in Figure B.6 to see lower frequencies more clearly and zoomed in Figure B.7 to distinguish high frequency. 50 Hz mains interference overlaid with RF noise can be recognised from the images. In addition, ca. 100 mV AC could be measure with a multimeter.

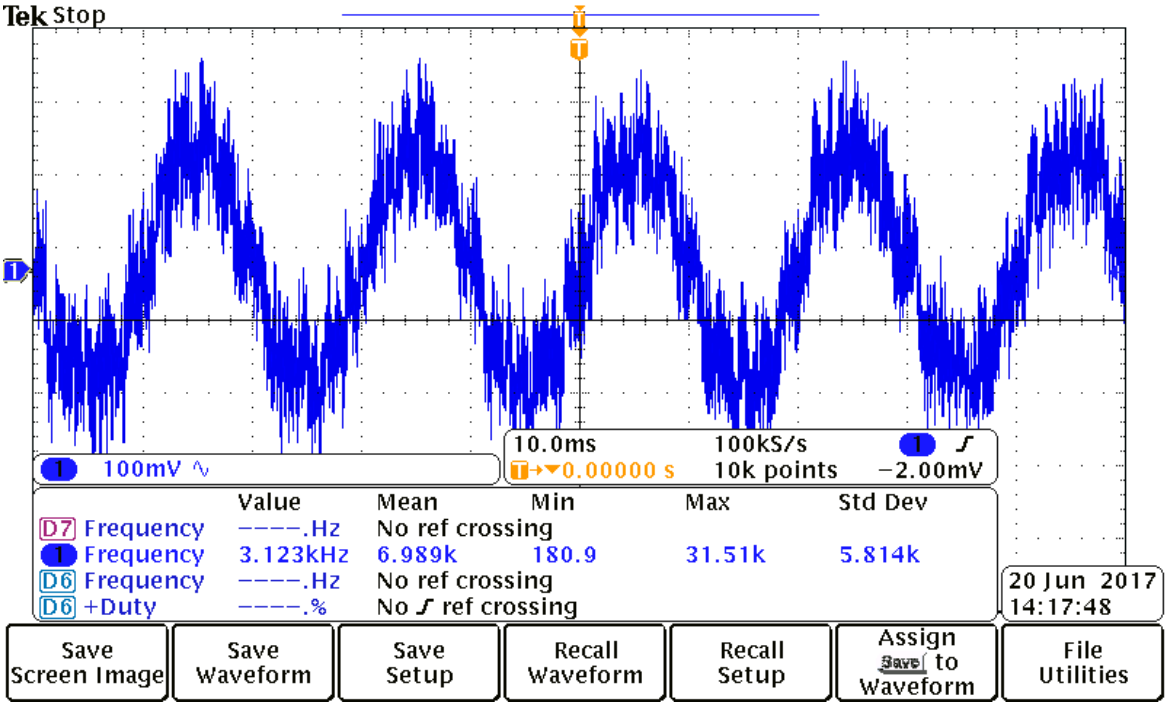

Figure B.5.: Oscilloscope probing of an 1.8 m open cable, full bandwidth

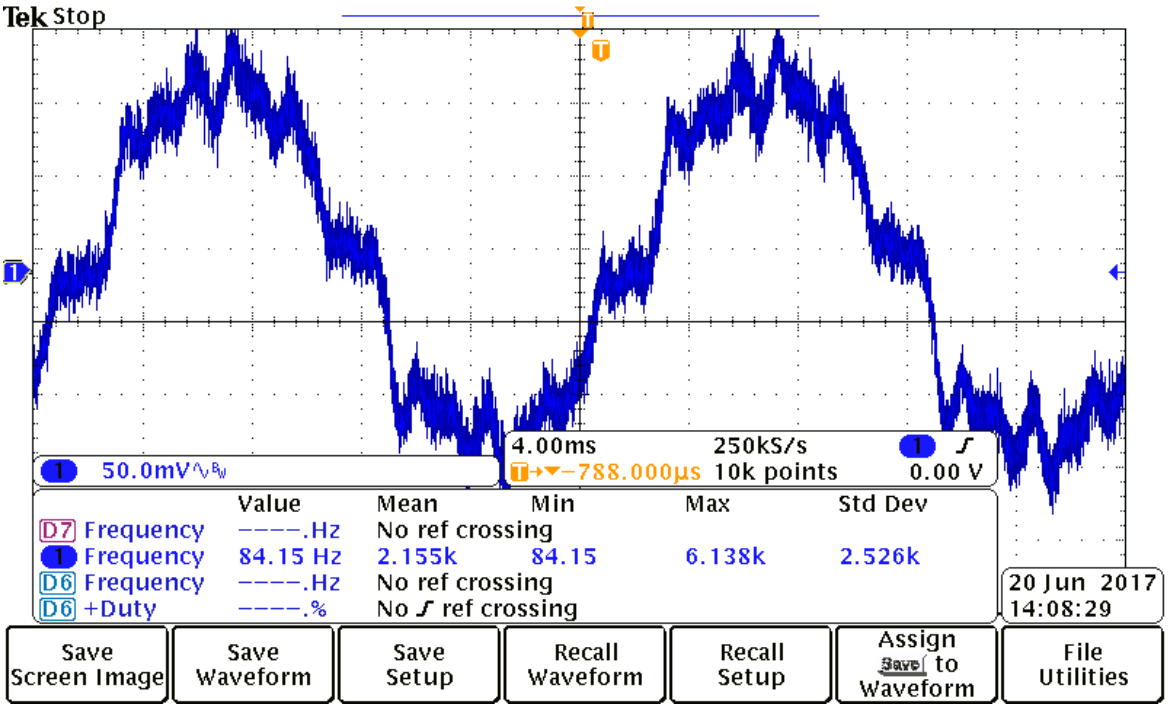

Figure B.6.: Oscilloscope probing of an 1.8 m open cable, 20 MHz band limit

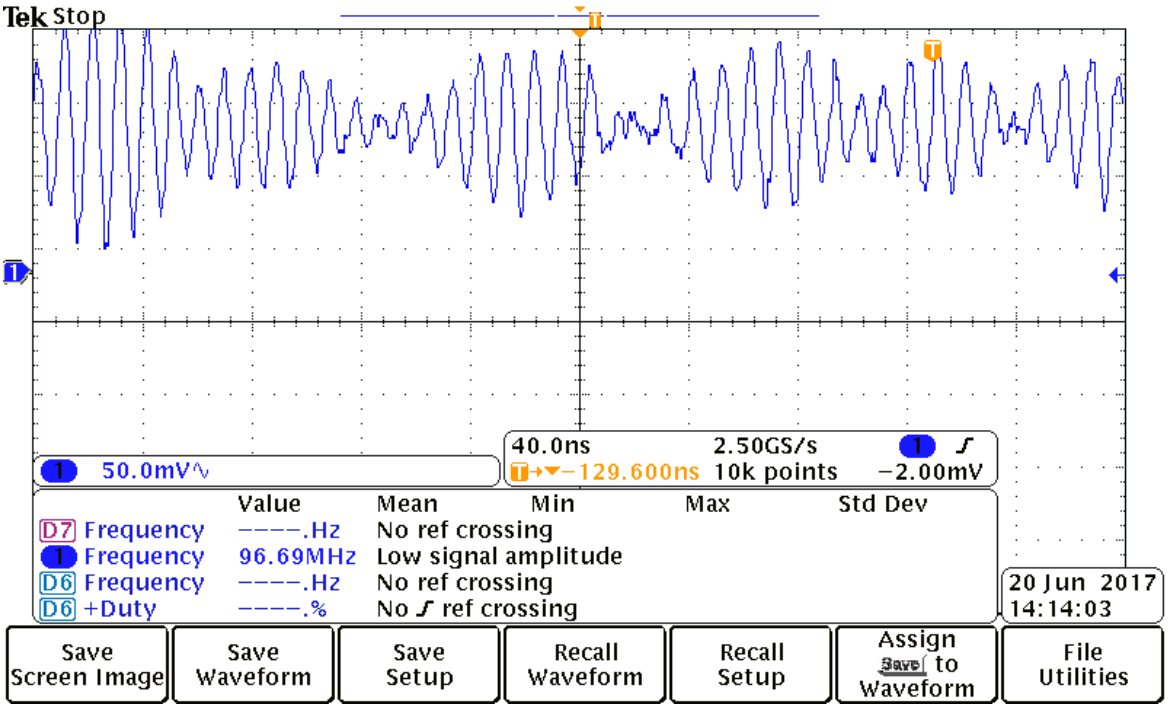

Figure B.7.: Oscilloscope probing of an 1.8 m open cable, zoomed in time

B.2. DAC

B.2.1. Prototype

The DAC was assembled on a prototyping board (Figure B.8). Since the pitch of the DAC is smaller than the pitch of the board, it was mounted on an adapter board. LT3042 provided 5.49 V power supply and LT6655B 5 V reference voltage. Both were mounted on adapter boards too. The board was also used in development of the control software for the DAC. Two tests were performed: linearity test and current capacity test.

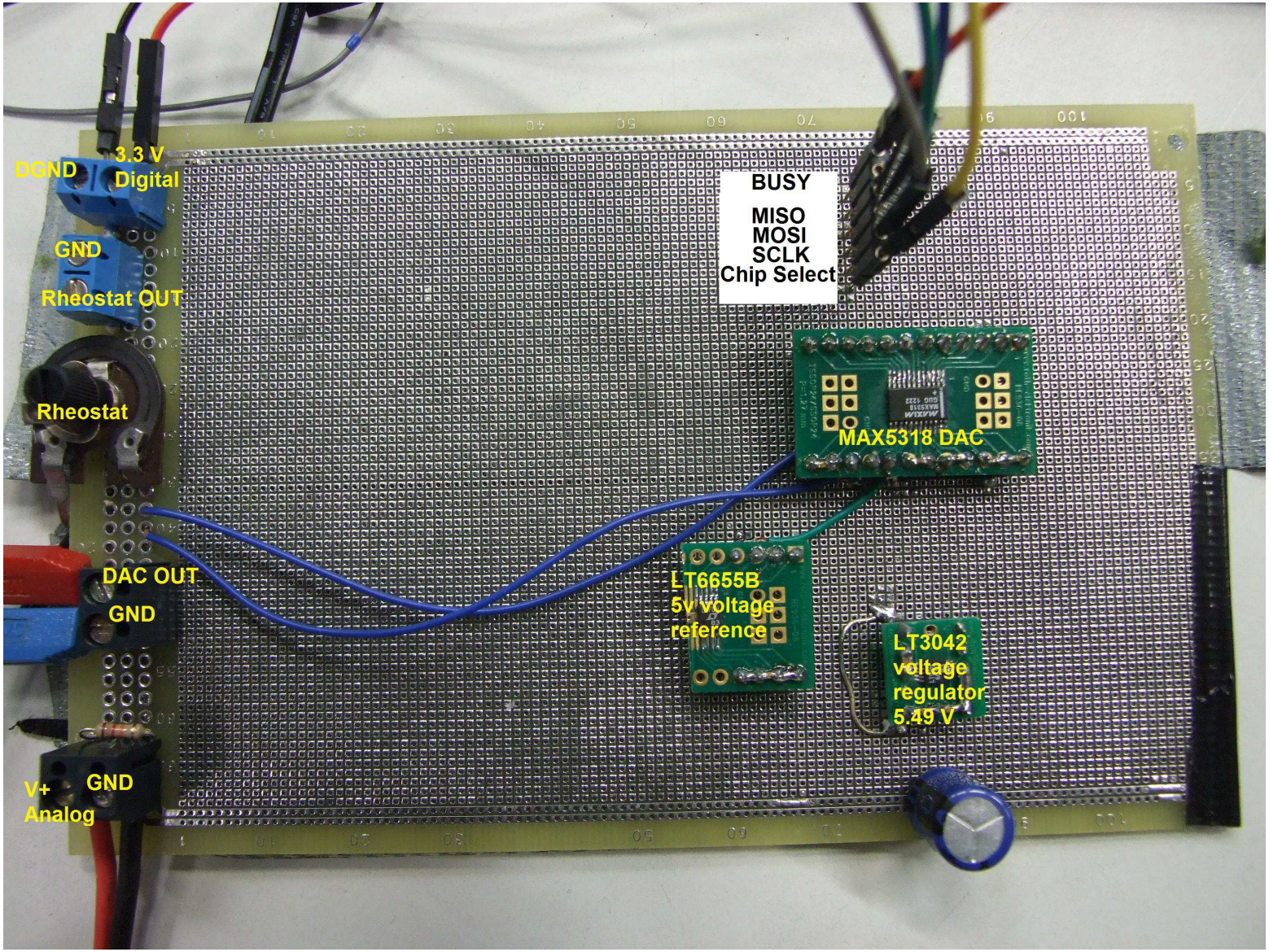

Figure B.8.: Prototype board used in the test of the MAX5318 DAC

B.2.1.1. Linearity Test

The linearity tests the performance of the ADC. It was performed by stepping through all codes of the ADC and measuring the output with Tektronix DMM4020 digital multimeter. The results and difference to ideal values were recorded. They are plotted in Figure B.9. Both offset and gain errors are noticeable. The apparent noise is due to insufficient precision of the DMM4020 in the range above 2 V. That is why no correction of errors was attempted.The DNL and INL could not be determined for the same reason. While the offset seemingly stays relatively small, the DAC demonstrates significant non-linearity at output voltages below 10 mV (Figure B.10). This happens due to lower limit of the voltage swing of the internal output buffer amplifier.

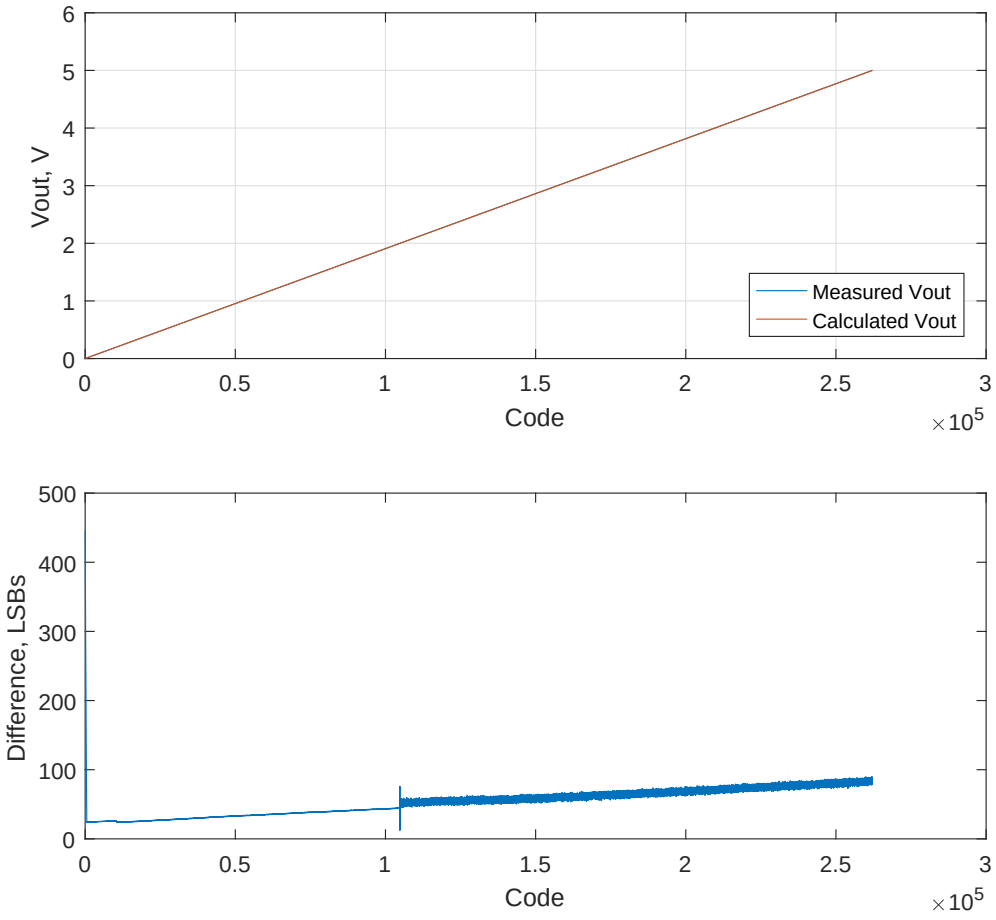

Figure B.9.: Plot of DAC linearity test Apparent noise is due to switching of the DMM4020 range, which reduces the precision of the measurement.

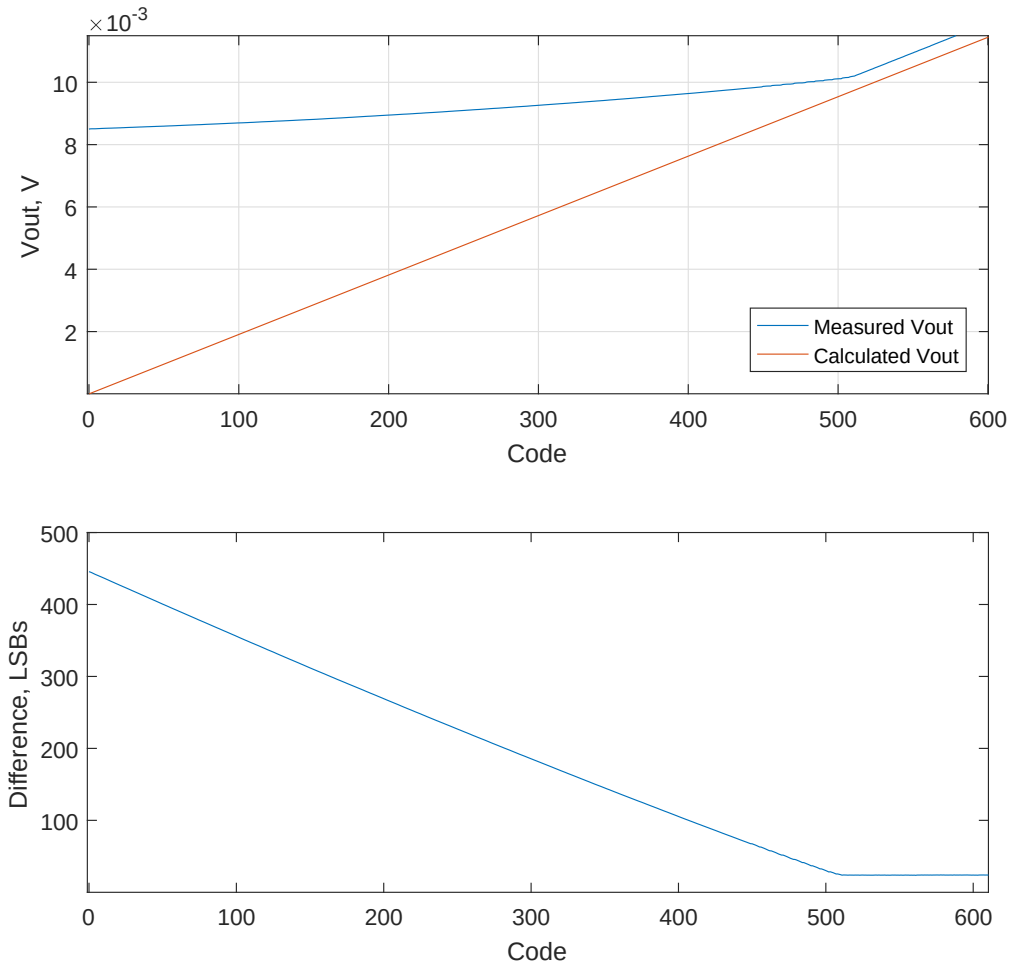

Figure B.10.: Plot of DAC linearity test with bottom left corner zoomed in. The non learity and offset error can be clearly seen.

B.2.1.2. Current Capability Test

The current capability test consist of sourcing and sinking. For sourcing test the DAC output was set to fullscale and connected to ground through a rheostat. For sinking test the DAC output was set to 0 V and connected to 5 V through the same rheostat. In both cases the rheostat with nominal resistance 4.7 kΩ was used to adjust current, which was measured by Tektronix DMM4020. The output voltage was measured by Fluke 45 multimeter and recorded in the process. The values are logged in Table B.1 and Table B.2 and plotted in Figure B.13.

Table B.1.: Current Sourcing Test. The circuit is shown in Figure B.11

Current, mA	$\mathbf{U_{out}}$**,** V
1.08	5
4.55	5
13.2	5
20.8	5
31	5
39	4.89
50	4.6
55.3	4.4
57.7	4.3
62.2	3.58
64.8	1.95

Table B.2.: Current Sinking Test. The circuit is shown in Figure B.12

Current, mA	$\mathbf{U_{out}}$**,** V
1.1	0.01955
5.19	0.077
10	0.148
20.6	0.32
32.5	0.58
36.2	0.73
38.9	1.08
39.5	4.02

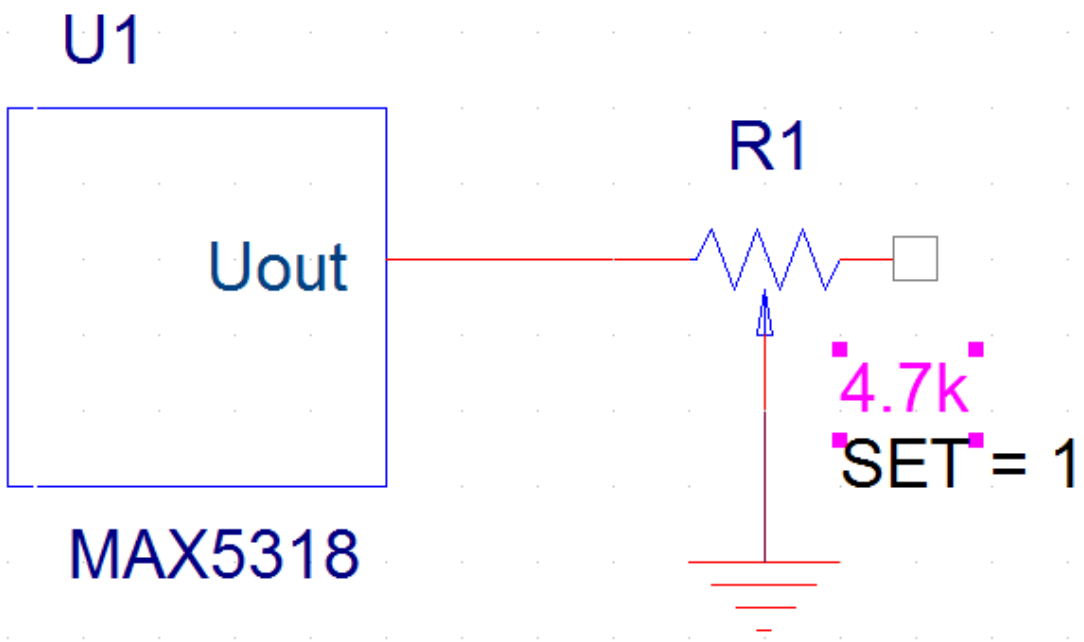

Figure B.11.: Principle circuit used in current sourcing test.

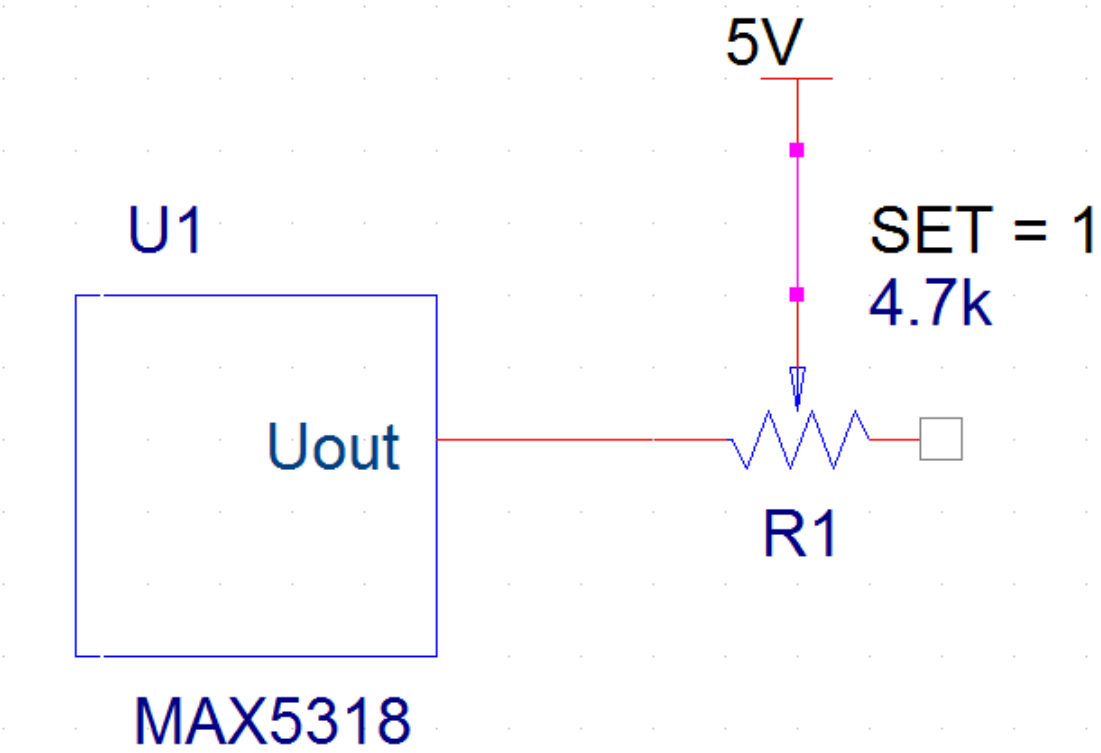

Figure B.12.: Principle circuit used in current sinking test.

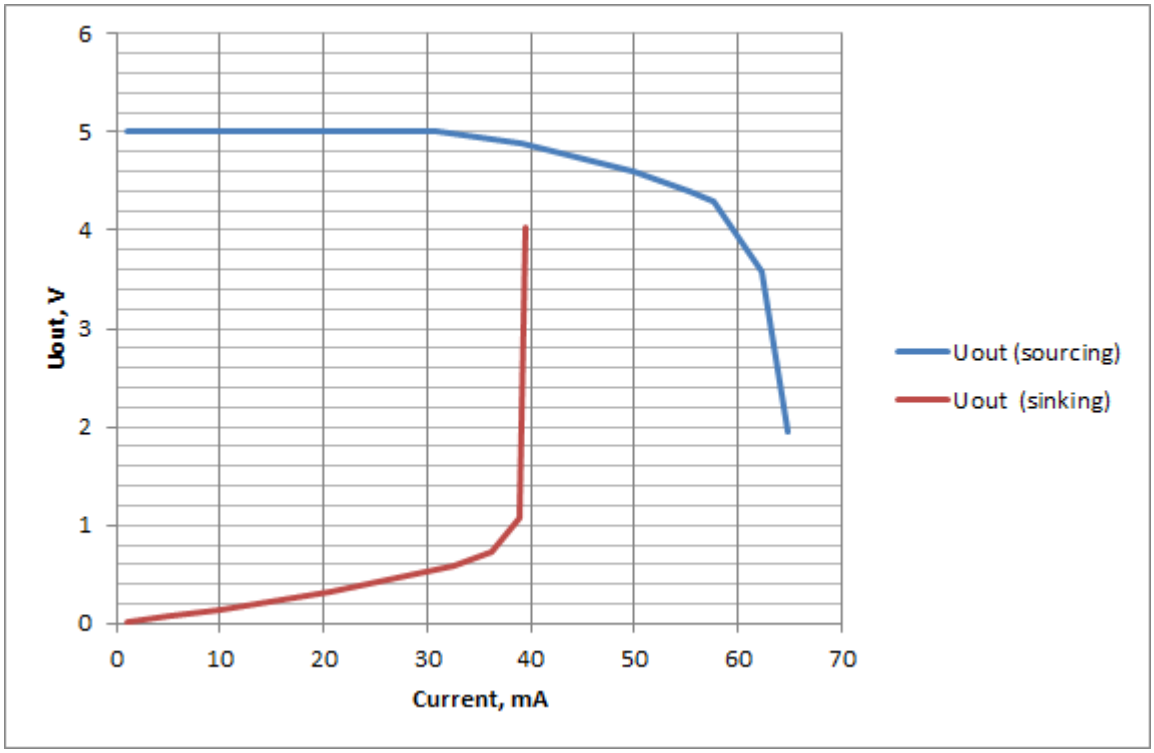

Figure B.13.: Chart of the current capability of the MAX5318 DAC.

B.2.2. Final assembly

The first test after the assembly was basic tests to set an output voltage, that was verified by multimeter, to make sure the DAC functions properly.

The final measurements of the MAX5318 DAC were performed by the onboard AD7175-2 ADC. This is legitimate, because the ADC has significantly higher resolution, which is, unlike the digital multimeters, is the same over full range of output voltages. The ADC was self-calibrated and set to 5 SP for maximum performance.

First the DAC was stepped through all codes. The voltage was measured and recorded along with difference to ideal output in volts and LSBs. The difference plot in Figure B.14 (top) shows obvious offset and gain errors.

The DAC, has however special offset and gain registers for correcting linearity errors. An attempt was made to make use of them. The correction,however can't be ideal for following reasons:

- The non-linear range at smaller codes (explained in Appendix B.2.1) prevents offset correction at 0 V. It was done at 15 mV.
- The DAC has gain error >1, which would cause the ADC to overflow. That is why some headroom is required to account for that. Ultimately the gain was corrected at 4.990 V.

The test was repeated after correction was performed. The plot in Figure B.14 shows the offset and gain were successfully calibrated out.

This opens possibility for a automatic calibration procedure of the measurement system: first the ADC is self-calibrated. Then it is used to calibrate the DAC.

Once the errors are corrected, it is possible to determine the integral non-linearity (INL) and differential non-linearity (DNL). They are plotted in Figure B.15 excluding first 600 codes in the non linear range. The sawtooth-like shape of the INL Plot and apparent spikees in DNL are very likely artefacts of digital correction of the linearity errors (see [40]).

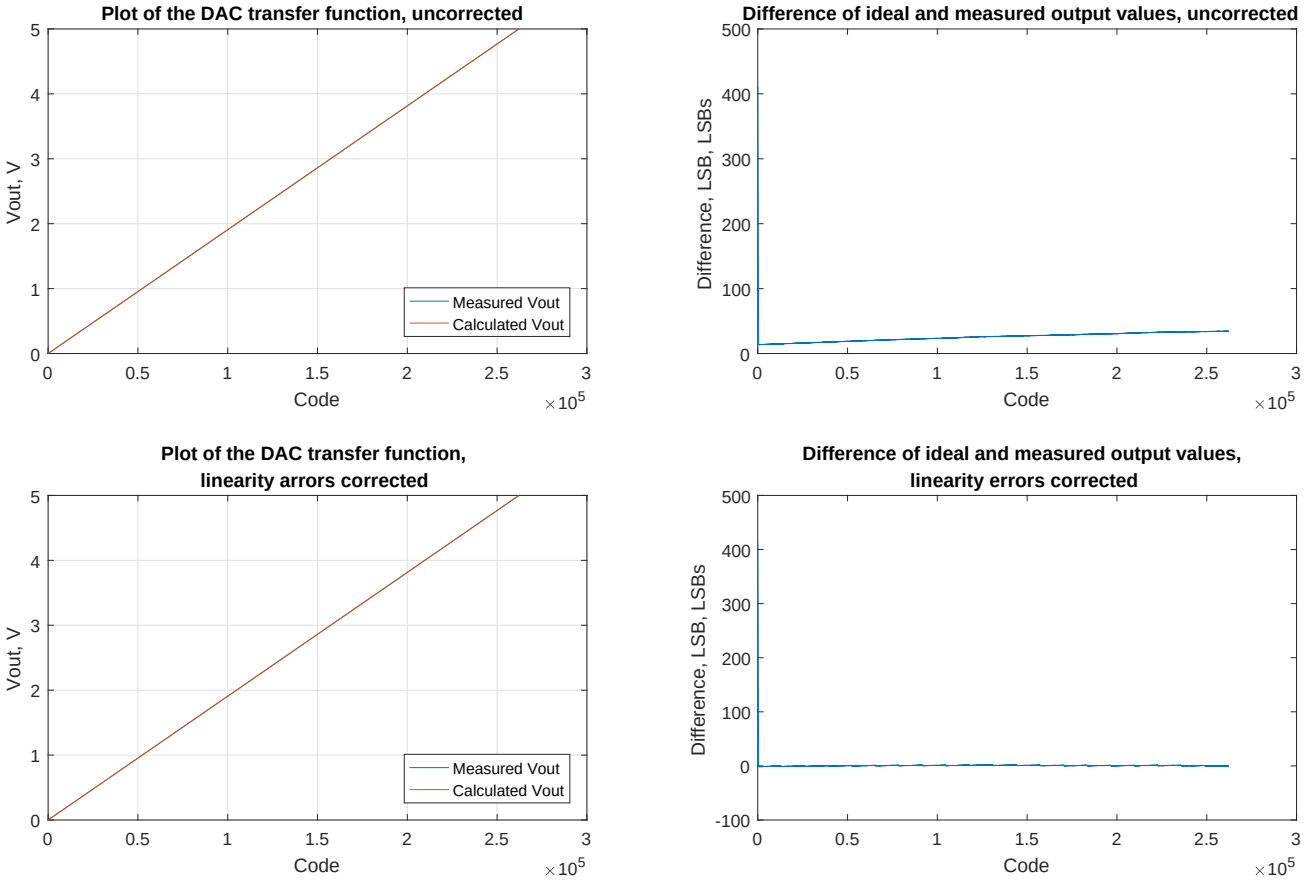

Figure B.14.: MAX 5318 DAC transfer plot, comparison of uncorrected and corrected linearity errors

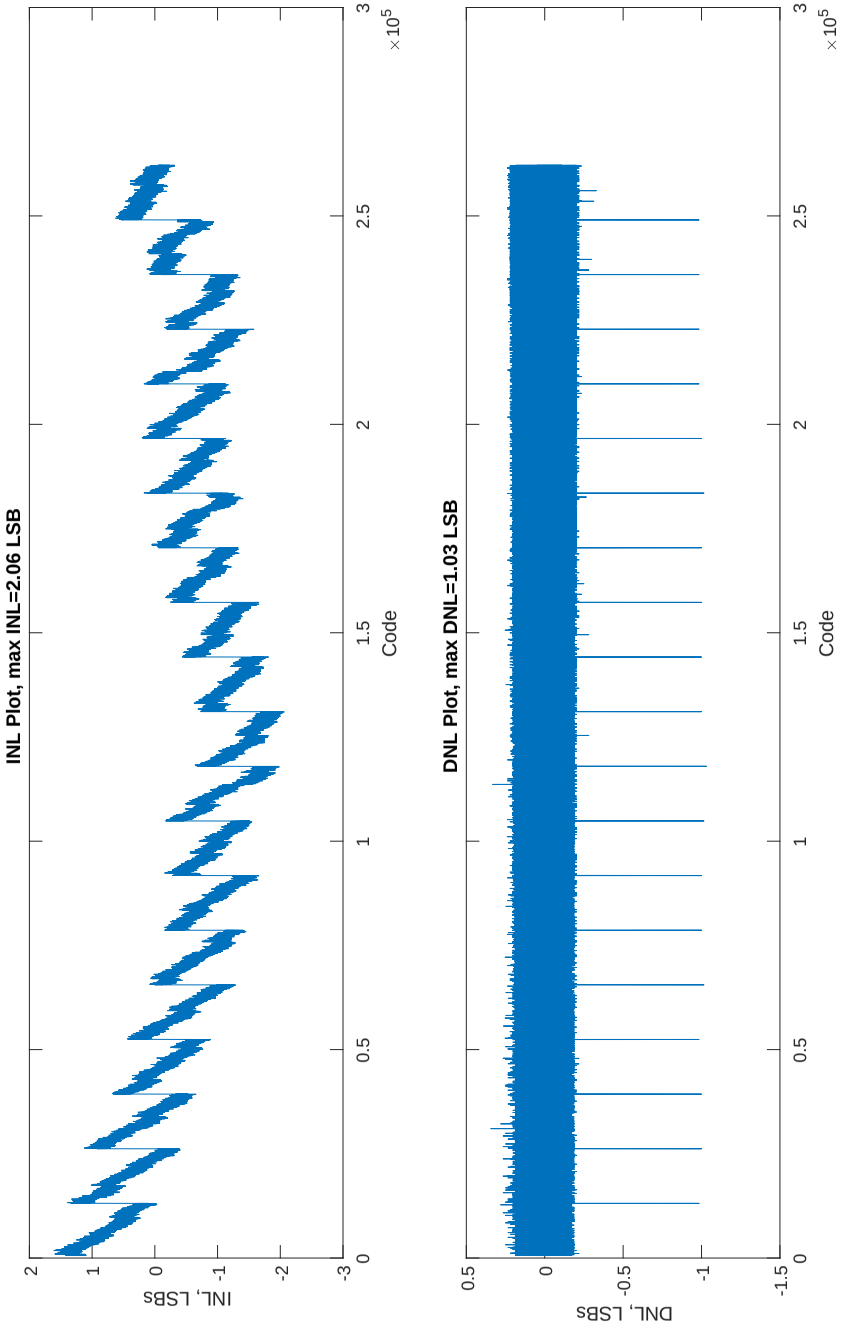

Figure B.15.: Plot of the INL and DNL of MAX5318 DAC

B.3. ADC

B.3.1. Prototype

The modified DAC prototype was used for ADC testing. Before showing the testing results, the features of the AD7175-2 ADC and testing methodology have to be presented first.

AD7175-2 is a sophisticated 24-bit Δ-Σ ADC. It has four logic channels and setups.Five analog inputs may be arbitrarily assigned to channels. The ADC offers wide range of data rates selectable separately on each channel. Optional input and reference buffers are also included. The choice of filter consists of sinc3 and sinc5 filter. The latter may be additionally supplemented by an enhanced 50 Hz+60 Hz filter. A very useful feature is unipolar mode, when the positive differential voltage is converted with full 24-bit resolution. A 2.5 V reference the can be activated on channel-by-channel bases is also included. This opens possibility to use internal reference for current measurement, thus bring ing it closer to ideal range and potentially increasing precision. (Figure B.16). The ADC inputs were assigned as following on the prototype:

ADC input	Function
AIN0	DAC pole of the shunt resistor
AIN1	Battery side of the shunt resistor
AIN2 and AIN3	Battery voltage. The poles can be set in software
AIN4	Ground

The bias currents of the input buffers were measured at 15 nA during active conversion and were non-measurable, when inputs were deactivated.

During conversion the channels are processed sequentially. That is the reason for default output data rate of 100 SPS chosen for all tests, unless specified otherwise. It can be more easily explained in terms of conversion times. The measurement on a battery typically require two channels for voltage and current. The conversion time for ODR 100 SPS is 10 ms. Assuming same data rate on both channels, total conversion time on both channels is 20 ms, corresponding to 50 SPS output rate, which is demanded by the specification.

Following conversion modes are available:

- Single conversion. User has to request each conversion
- Continuous.The channels are converted continuously in a cycle.

Moreover, there are three self-calibration procedures, that may be performed separately for each channel:

- Internal offset calibration
- System offset calibration
- System gain calibration

System calibration require external application of certain voltages to pins and thus impossible to perform only in software.

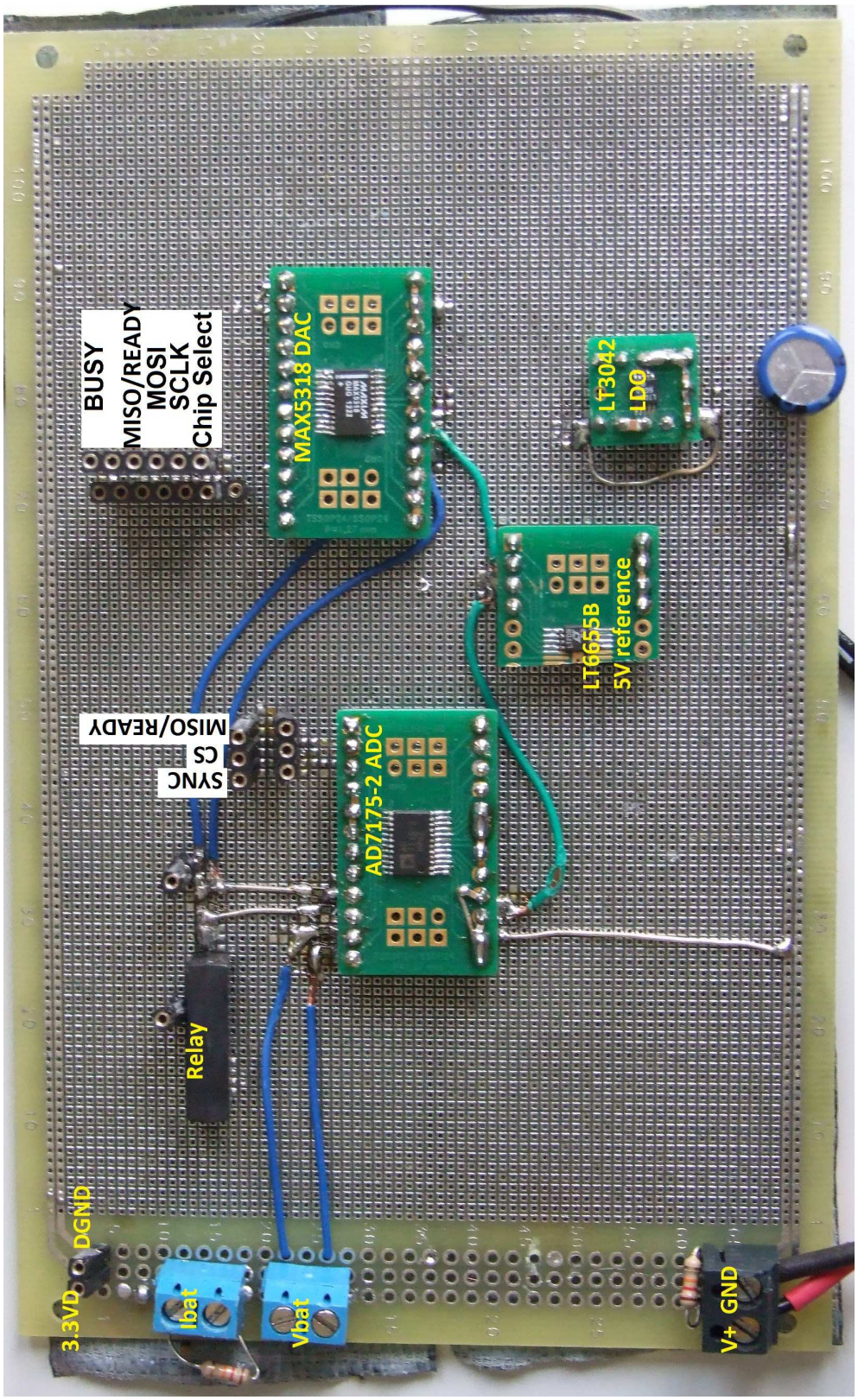

Figure B.16.: The prototype used in the testing of the ADC. The relay is SIL03-1A72-71D. The pins were duplicated to allow the connection of a digital oscilloscope.

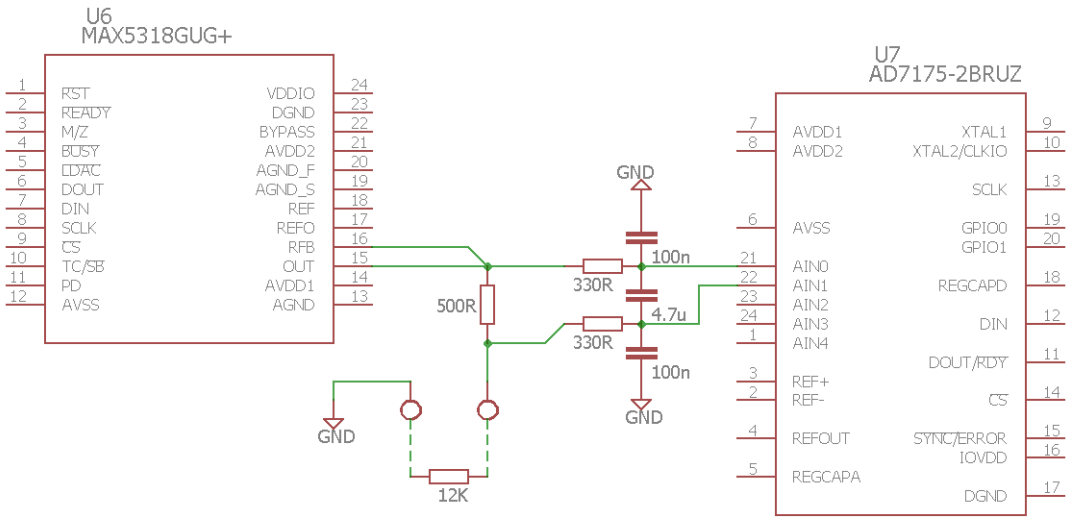

Figure B.17.: Principle diagram of the circuit used in noise testing. The AIN0 input was shared between differential and pseudo-differential test.

B.3.1.1. Tests of Noise

The goal of noise test is investigation of stability of conversion results and influence of different settings on the performance of the ADC both for differential and pseudo-differential measurements. The voltage for the tests is sourced from the DAC. Pseudo-differential tests directly measure its voltage, while differential tests measure voltage over shunt resistance, which is produced by connecting a 12 kΩ resistor externally in place of a battery. This voltage correspond to current, if divided by shunt resistance. For all test the input buffers are enabled, the output dtat rate is set to 100 SPS and 10000 conversions are performed. 100 SPS chosen to achieve 50 SPS mandated by specification in two channel (current and voltage) operation. The circuit used in this test is depicted in Figure B.17.

The results are presented as plot of measured voltage and histogram of codes. The range and standard deviation of noise (equals to RMS noise) as well as code spread on counts and noise free resolution are calculated.

Settings that were investigated and conclusions from them:

List of noise tests

Measurement type	**Measurement**	**Figure**	**Conclusion**
Pseudo-differential measurements	Single vs continuous conversions	B.18	The contious is distorted by a few outliers, otherwise they roughly equal.
	Sinc3 filter vs sinc5 filter + single channel vs two channels	B.19	Sinc5 looks slighly worse in single channel due to a few outliers. In two channel mode the filters show similar performance. However, during testing it was overlooked that sinc3 triples its conversion time in multichannel operation. Therefore sinc5 filter is preferable for such function.
	100 SPS vs 16.66 SPS vs enhanced filter	B.20	This test checks what could be gained by reducing data rate and enabling the enhanced 50/60 Hz filter. Only small gain from speed reduction and barely any benefit from the enhanced filter.
Differential measurements	Single vs continuous	B.21	Both modes have almost identical performance. Also strong improvement over pseudo-differential measurements strikes out.
	Internal vs external reference	B.22	Considering different full-scale, the performance is similar
330 Ω vs 33 Ω filter resistors	Pseudo-differential	B.23	Slight performance degradation is noticable with 33 Ω resisto
	Differential	B.24	The performance degradation is consistent with pseudo differential measurement.

Based on this results, following configuration was selected as default: SINC5 filter, data rate 100 SPS. The initial filter configuration is to be kept. However, final conclusions can be made after tests of the final assembly.

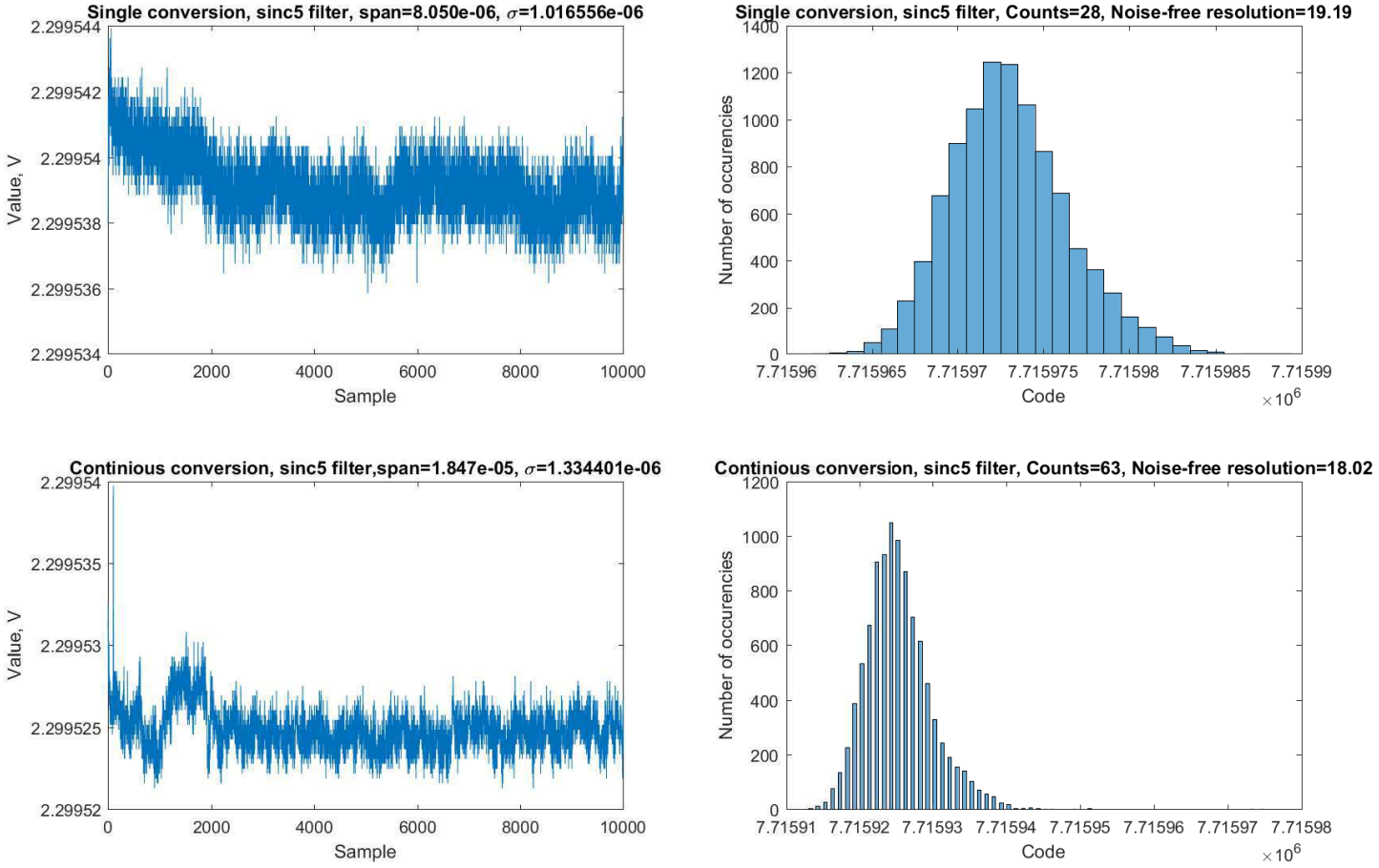

Figure B.18.: Comparison of single conversion vs continuous conversion, pseudo-differential measurement.

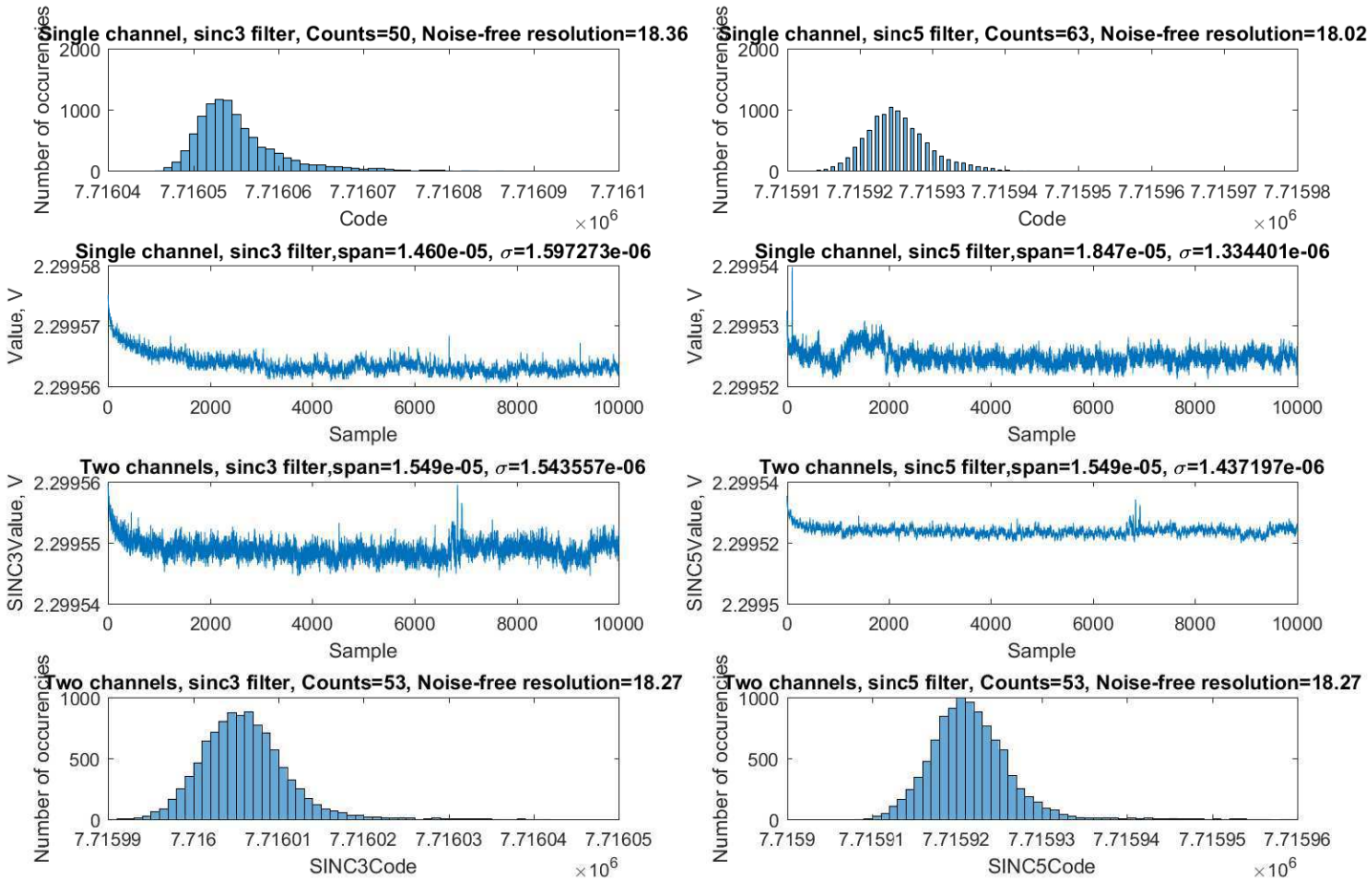

Figure B.19.: Comparison of sinc3 and sinc5 filters in single and two channel operation, pseudo-differential measurement.

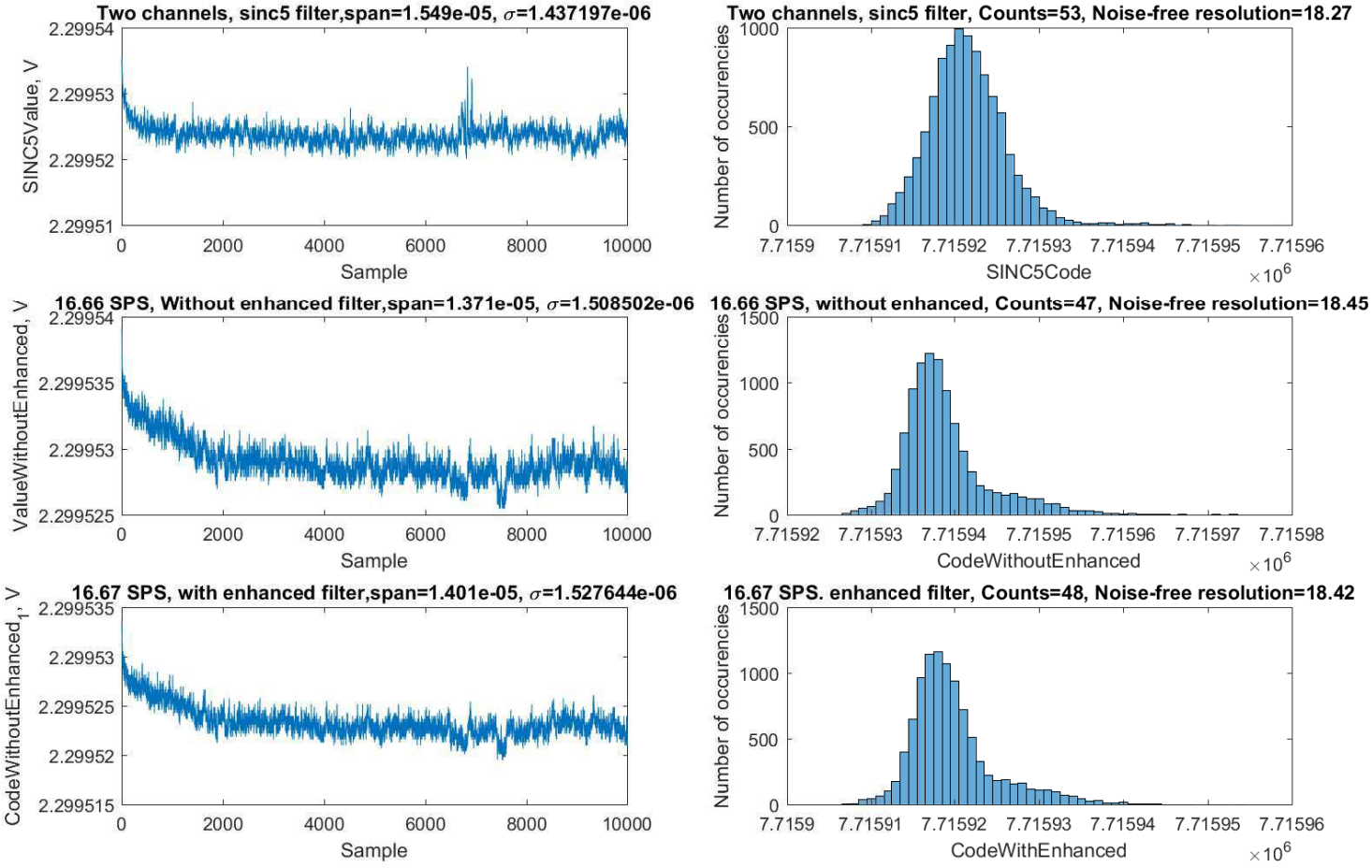

Figure B.20.: Comparison of 100 SPS with 16.66 SPS and 16.67 enhanced filter, pseudo-differential measurement.

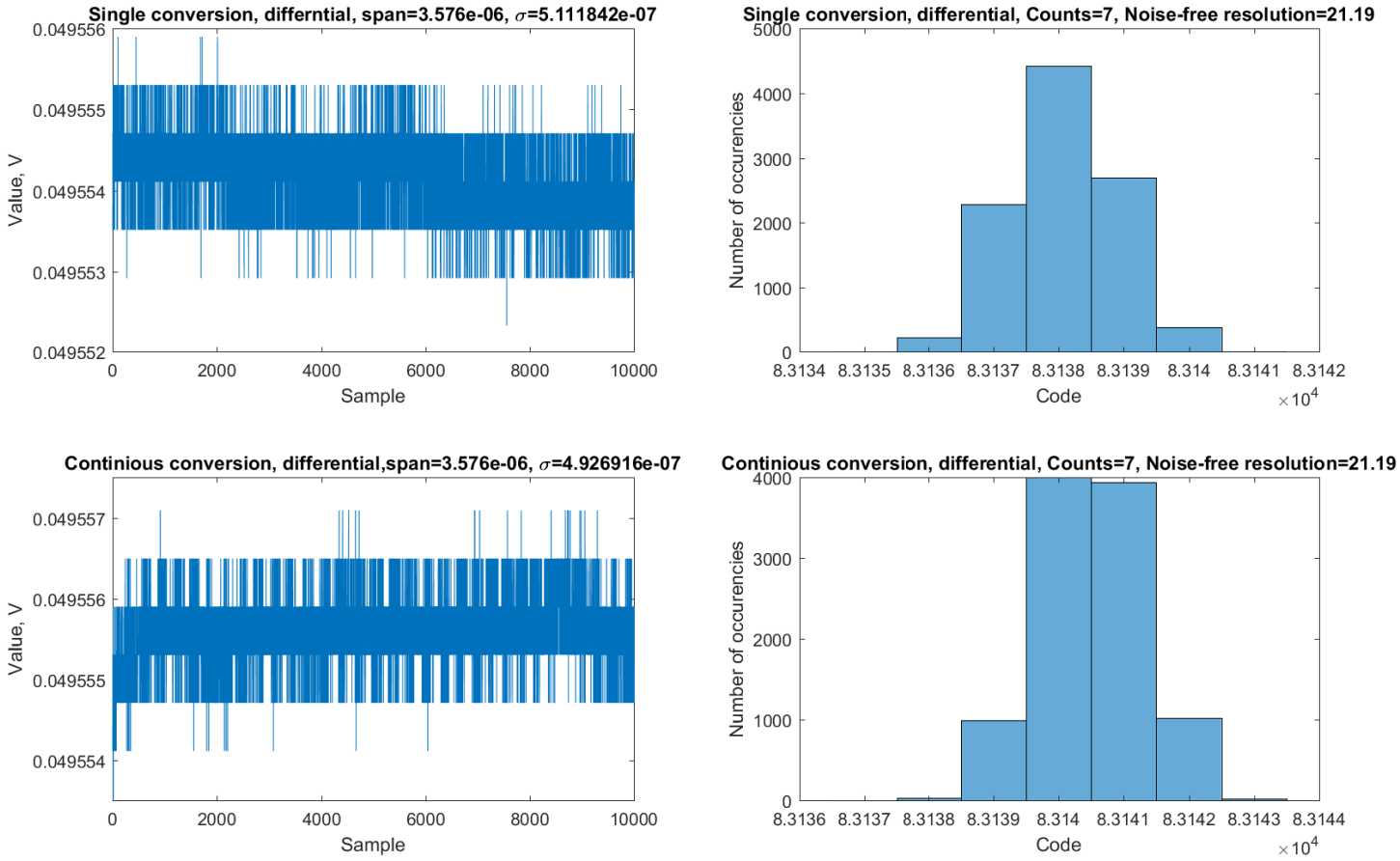

Figure B.21.: Comparison of single conversion vs continuous conversion, differential measurement.

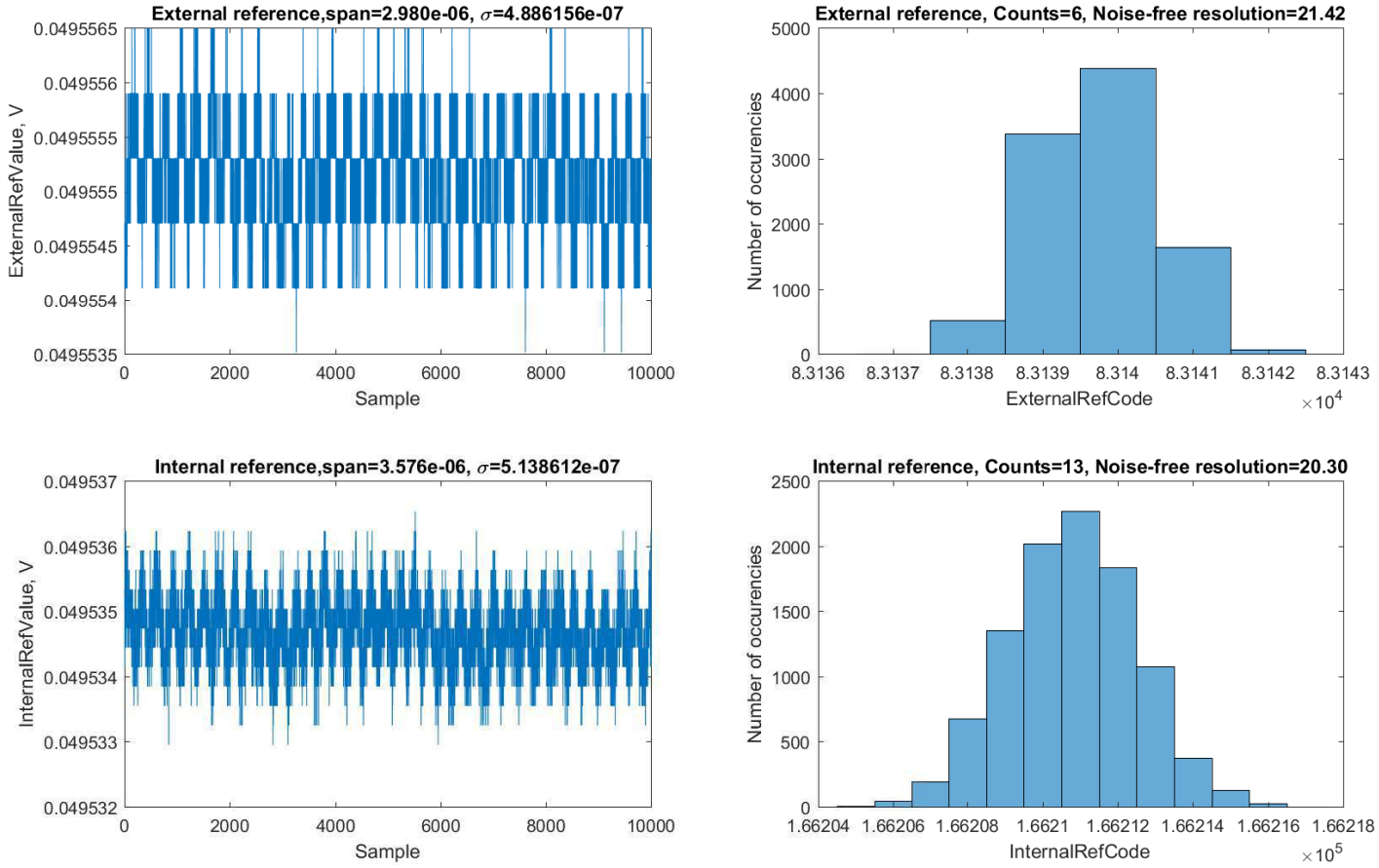

Figure B.22.: Comparison of external and internal voltage references, differential measurement. Note, that internal reference is 2.5 V, while external 5 V. Therefore LSB with the internal reference is half of the external.

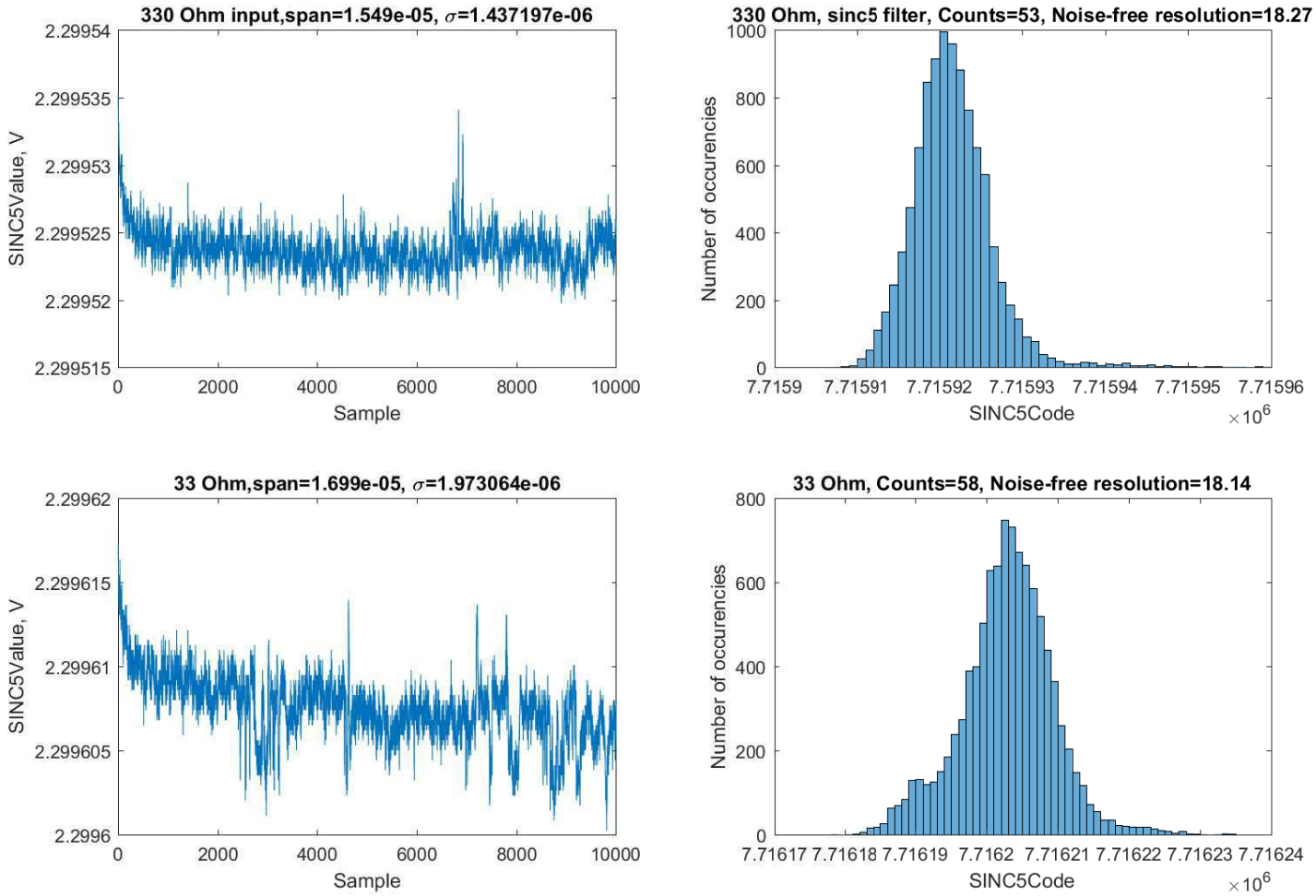

Figure B.23.: Comparison of 330 Ω and 33 Ω input resistors, pseudo-differential measurement

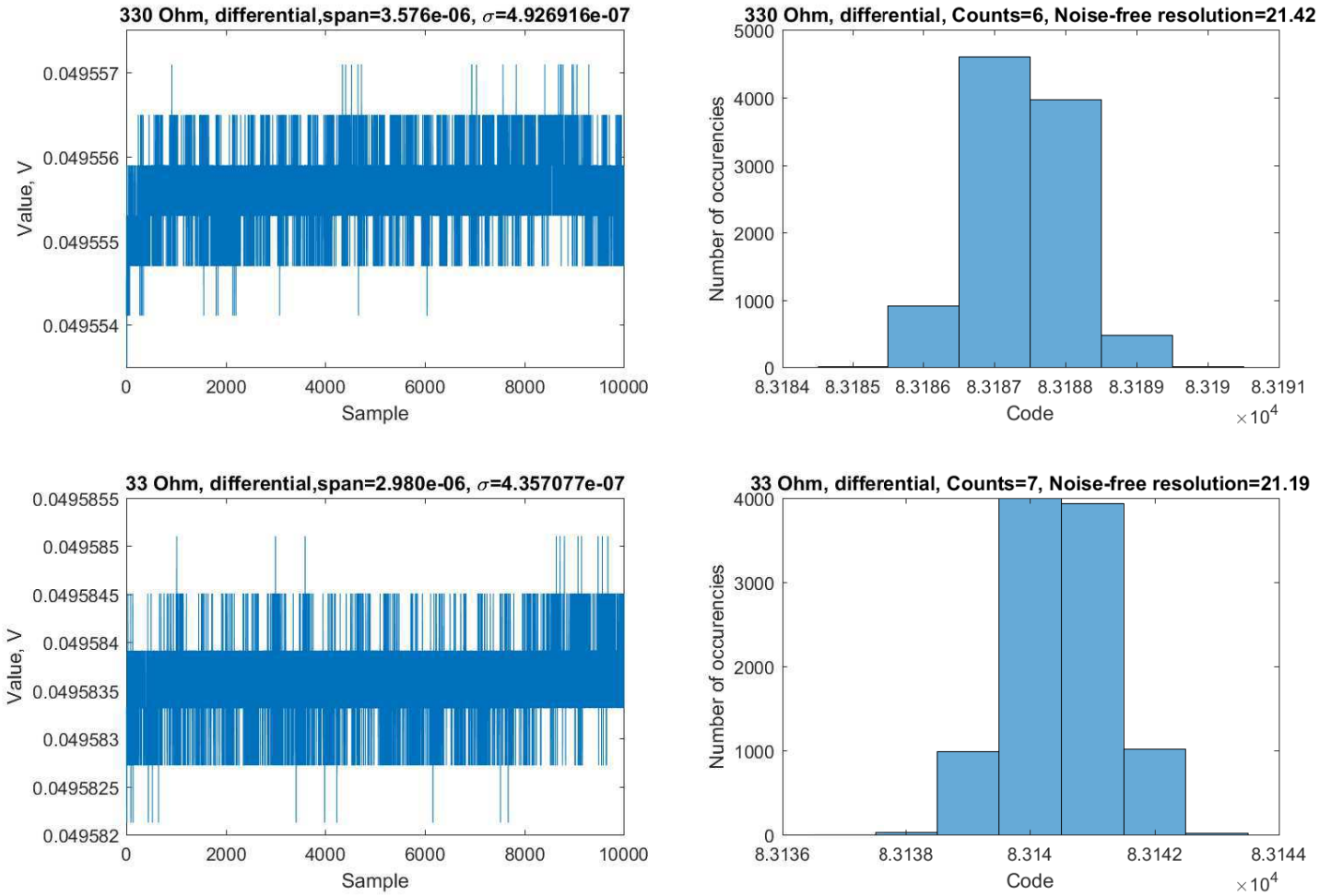

Figure B.24.: Comparison of 330 Ω and 33 Ω input resistors, differential measurement

B.3.1.2. Accuracy Tests

Accuracy of measurements is determined by comparing with Tektronix DMM4020. Two channels were active, one calibrated and other uncalibrated which enable direct comparison of the benefit of self-calibration procedures. Same circuit was used as noise testing (Figure B.17) with additional connection of the multimeters.

The pseudo-differential tests involves stepping through 500 voltage levels between 0 and 5 V by the MAX5318 DAC and measuring them by the AD7175-2 ADC and the DMM4020 multimeter.

Differential tests measured current through shunt resistor. Internal reference was used during these tests.

The precision of the multimeter depend on currently active range. This means that under circumstances the ADC may have better precision than Tektronix.

List of accuracy tests.

Test	Figure	Commentary
Pseudo-differential with offset calibration	B.25	Slight improvement of accuracy can be recognized.
Pseudo-differential with offset and gain calibration	B.26	Gain brought no apparent improvement over Figure B.25
Differential with offset calibration	B.25	This time the offset calibration brought measurement error from ca 170 nA to $\sim$50 nA
Differential with offset and gain calibration	B.26	o benefit from gain calibration is present.

The tests show relative high voltage measurement error, which may have been caused by the crudeness of the setup. On the other hand the current accuracy satisfies specification after offset calibration, which certainly should be used in future.

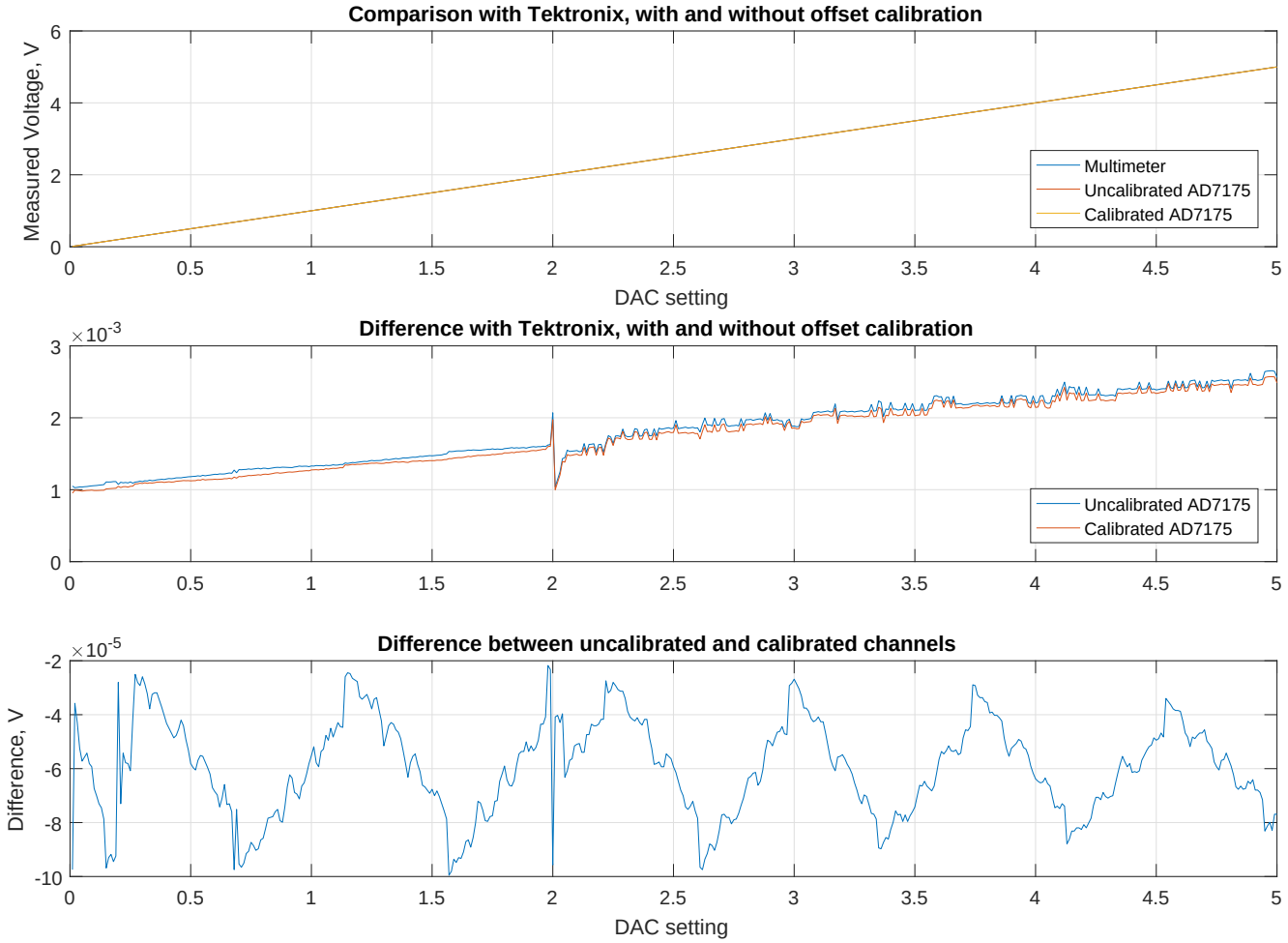

Figure B.25.: Pseudo-differential measurement with and without offset calibration. Note the DMM switching its voltage range at 200 mV and 2 V.

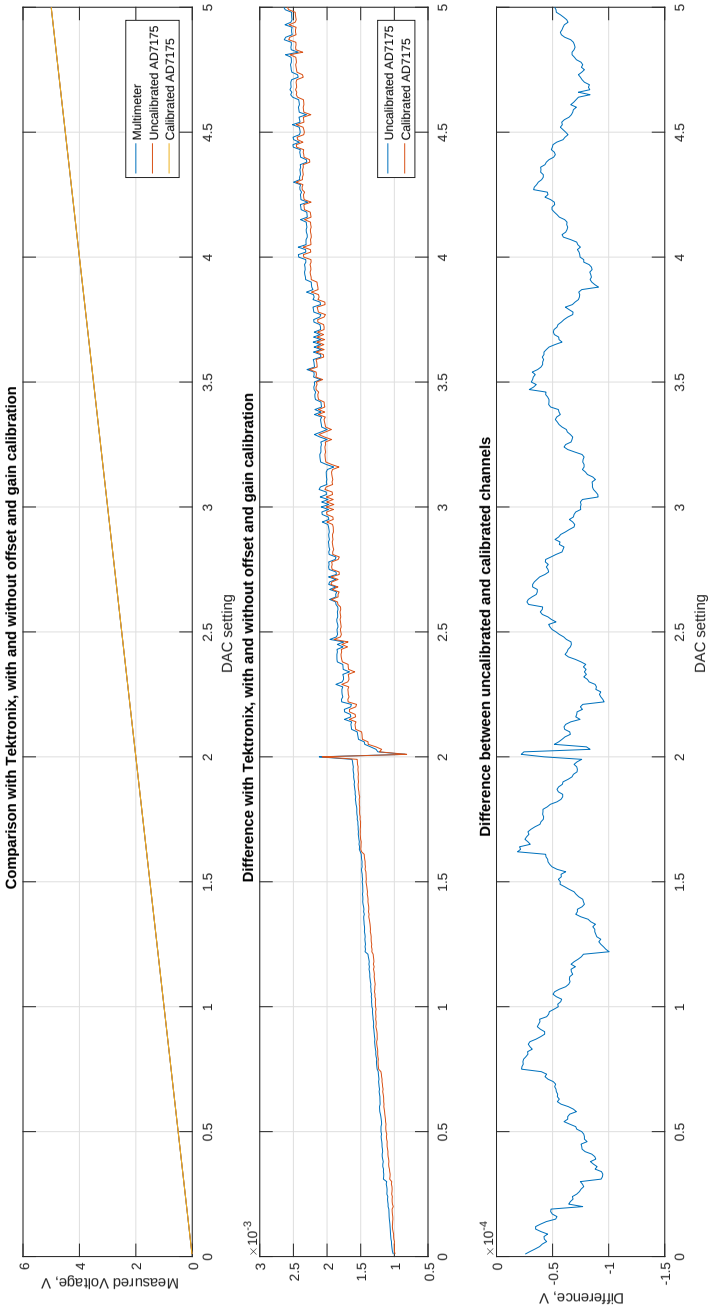

Figure B.26.: Pseudo-differential measurement with and without gain calibration. . Note the DMM switching its voltage range at 200 mV and 2 V.

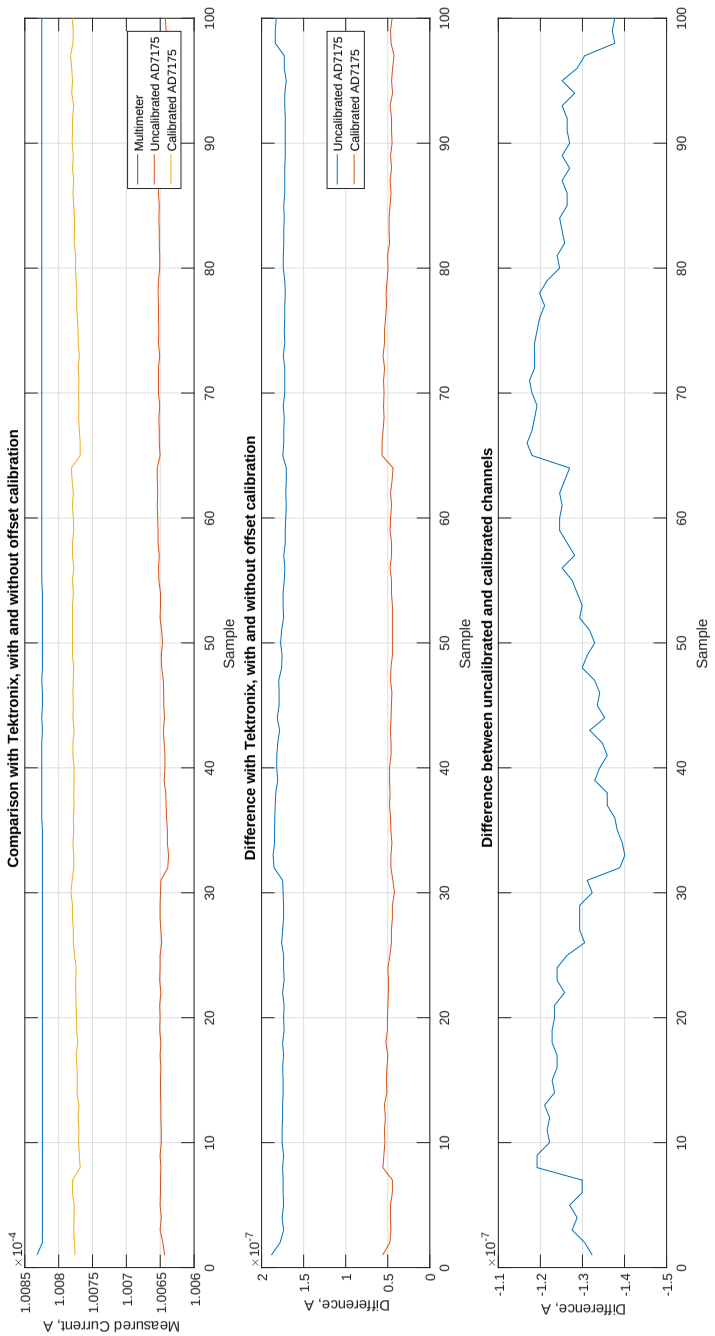

Figure B.27.: Differential measurement (expressed as current) with and without offset calibration.

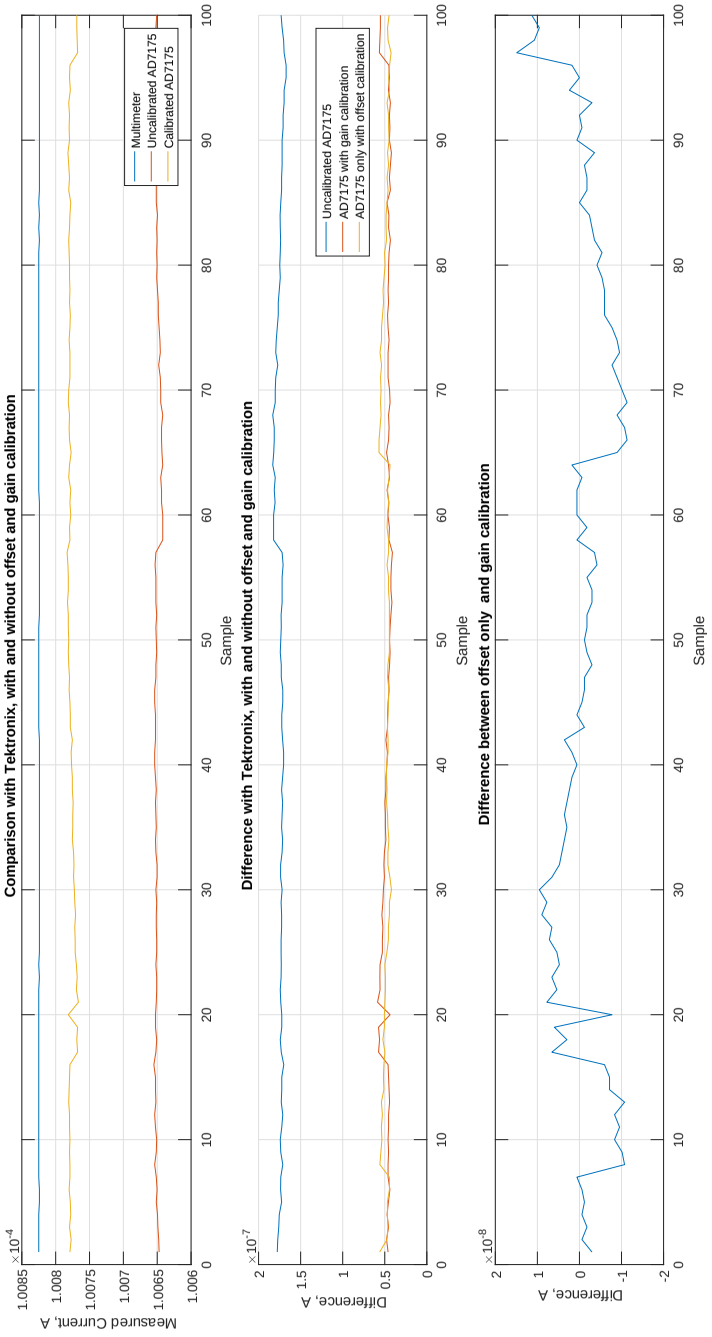

Figure B.28.: Differential measurement (expressed as current) with and without gain calibration.

B.3.1.3. Tests with Battery

Tests with battery serve getting impression of real world operation by charging and discharging a button cell. Since the current is not regulated, it happens in constant voltage mode. The tests are performed at first without multimeters to exclude any possible influence from them, then the current was measured by Tektronix DMM4020 and voltage with Fluke 45. However, it turned out that the multimeter have too low resolution at the tested voltage range. While looking on results one also should keep in mind that taking samples wasn't simultaneous. There is a varying delay between the DMM and the ADC.

List of accuracy tests.

Test	Figure	Commentary
Charging and discharging	B.29	The curves on charts are monotonic and smooth
Charging, compared with digital multimeter	B.30	The low resolution of the multimeters makes this measurement unreliable for voltage. The current roughly corresponds to what was determined ion accuracy tests.
Discharging, compared with digital multimeter	B.31	Same as charging

The voltage inaccuracy of $\approx$70 μV can be estimated from the sets. However, this is inconclusive due to low resolution of the multimeter. The current terst confirmed results from accuracy test.

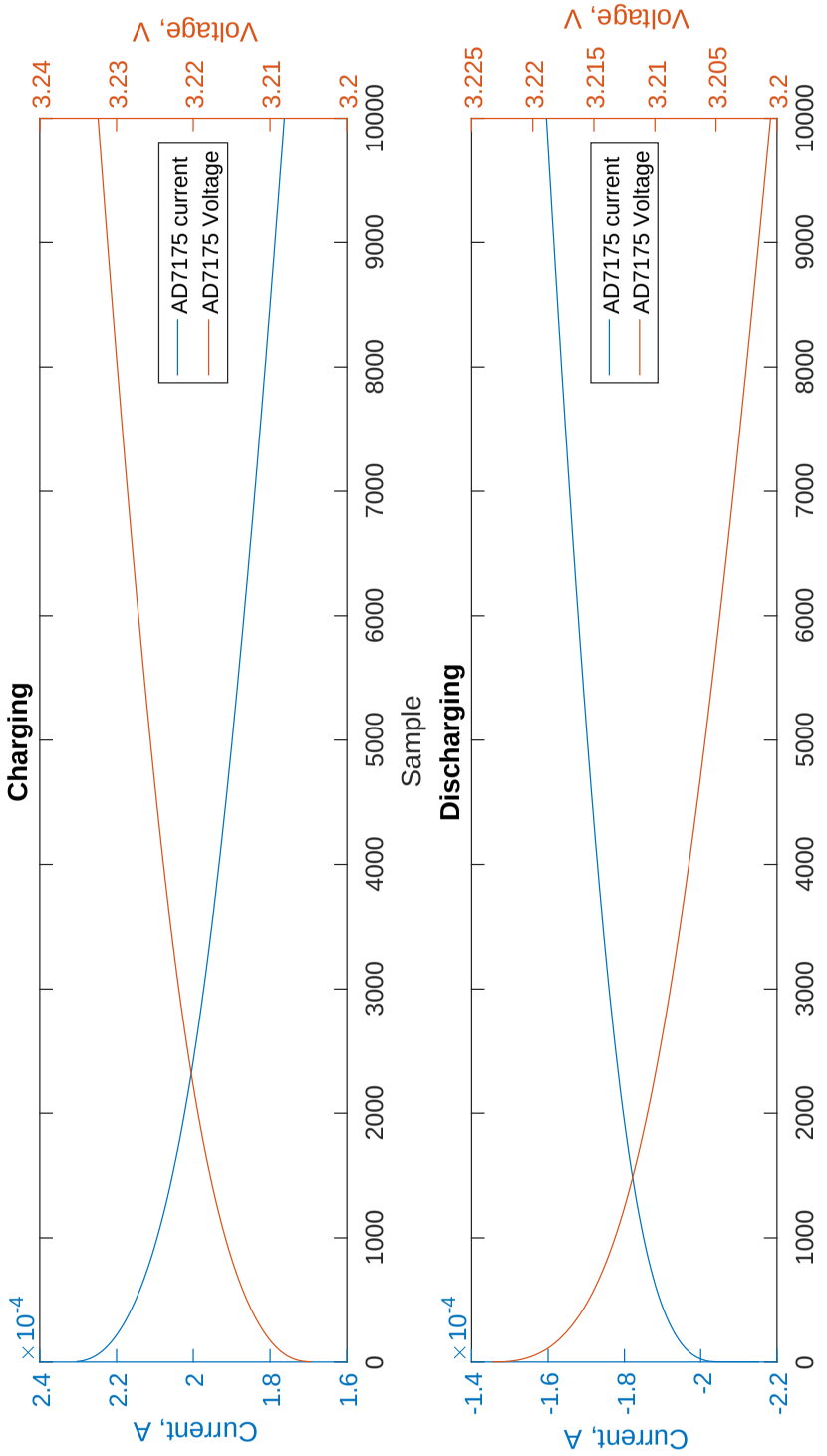

Figure B.29.: Charging and discharging of a button cell in constant voltage mode.

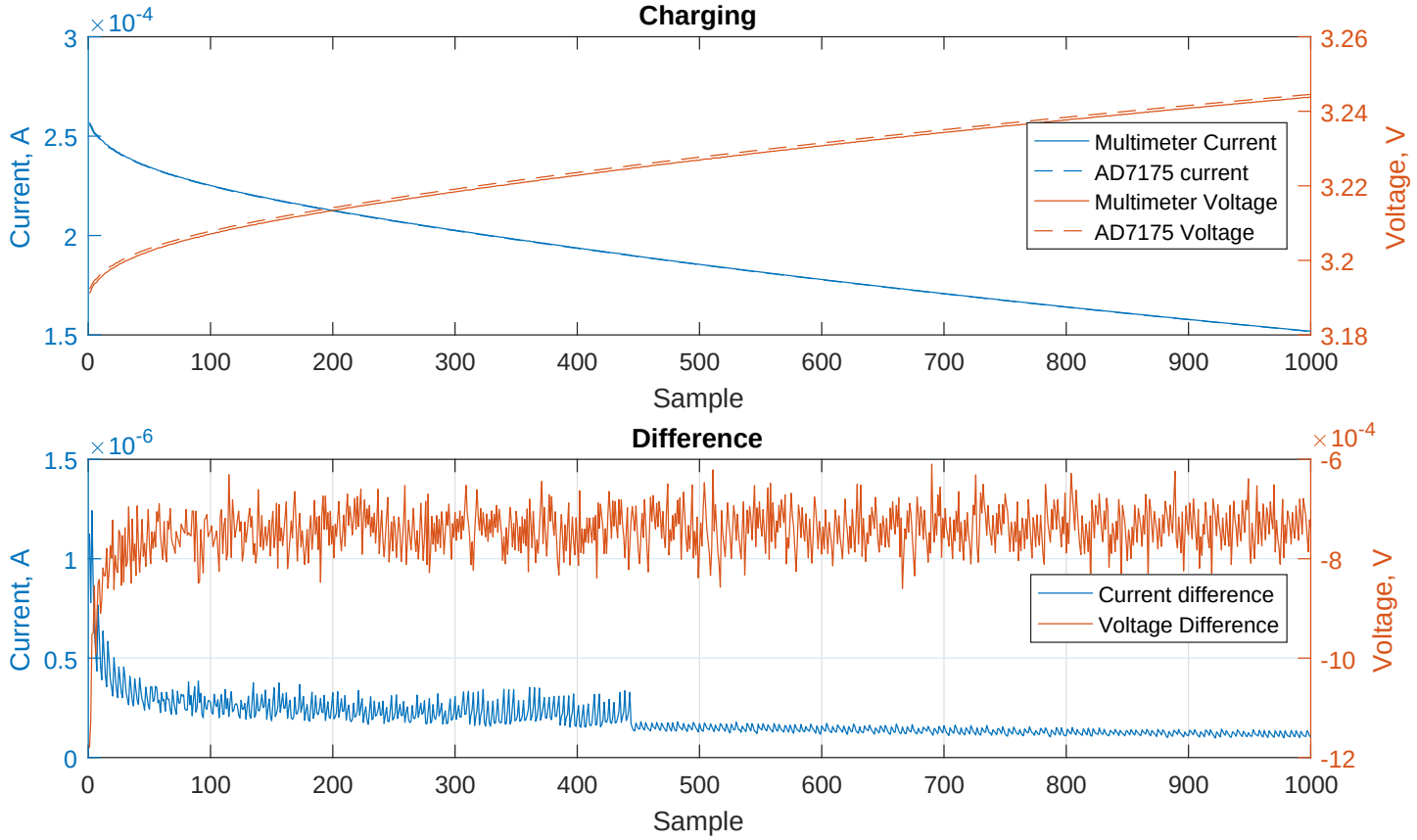

Figure B.30.: Charging of a button cell in constant voltage mode, compared with multimeters. Multimeters have low precision at measured values. That is how this apparent ripple came about. The current range was switched at 200 μA.

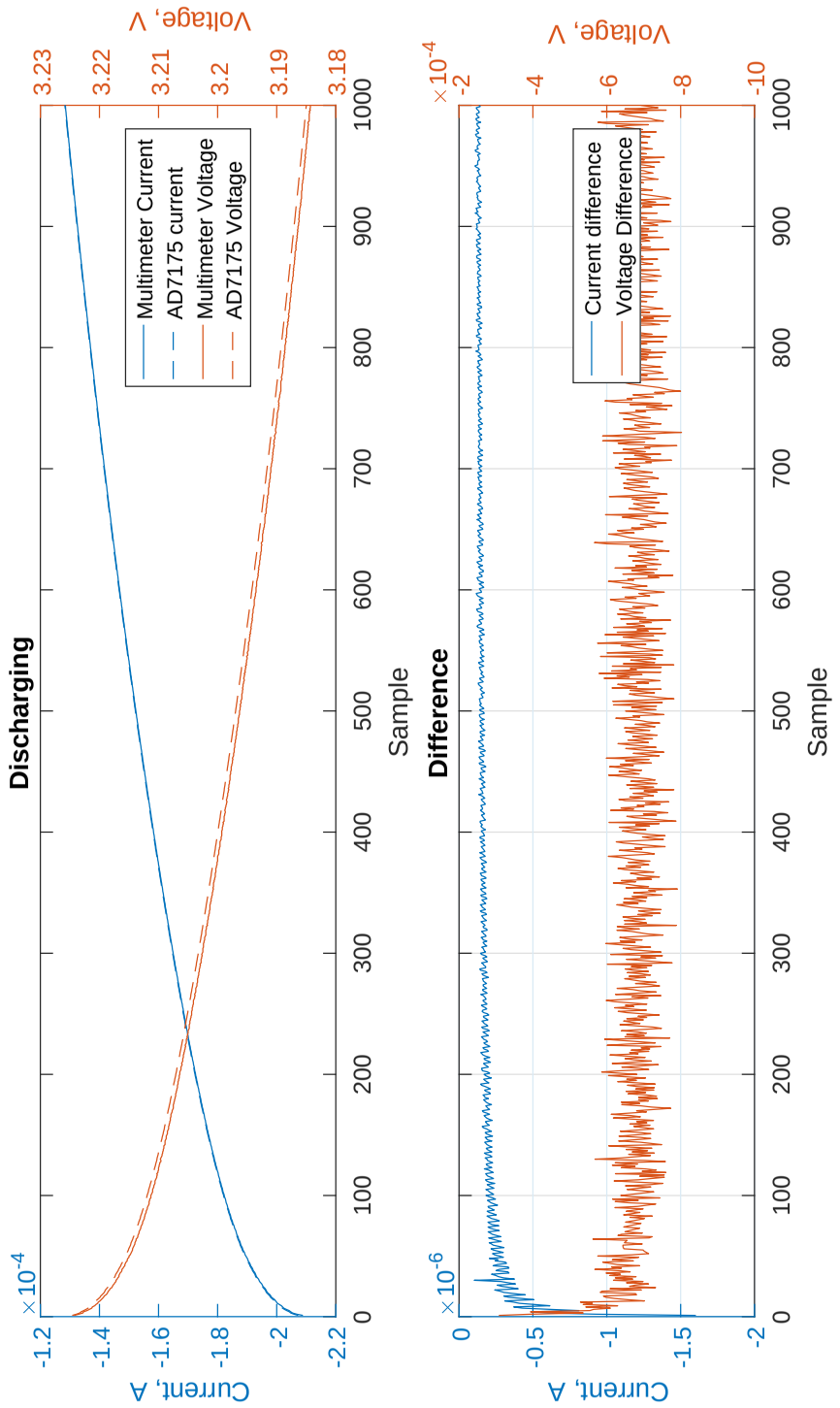

Figure B.31.: Discharging of a button cell in constant voltage mode, controlled with multimeters.

B.3.2. Final Assembly

The first test after the assembly was basic tests to gread some values from the ADC to make sure it functions properly.

B.3.2.1. Noise Test

These tests study *internal* noise of the PCB assembly and best real resolution of measurements. They are performed similar to those described in Appendix B.3.1.1 and use the same circuit (Figure B.17) to make them comparable to those tests. However, it is unnecessary to do one more extensive study of ADC configuration. Therefore, sinc5 filter was used for all tests. Three channel were active:

1. Pseudo-differential measurement of DAC output voltage.
2. Differential measurement over shunt resistor using external reference.
3. Differential measurement over shunt resistor using internal reference.

The two main comparison were made:

- Single conversion mode vs continuous mode
- Internal vs external reference.

Then the measurements were repeated at minimum data rate of 5 SPS to determine bsolute maximum performance.

The first tests were quite shocking. The noise performance was not better, if not worse than on prototype (Figure B.32, Figure B.33). However, the shape of noise didn't look white that suggested external source, probably the Raspberry Pi itself. Indeed, once the board was placed away from Raspberry Pi, the noise decreased dramatically. That means that the configuration with the board on top of Raspberry Pi is not suitable for measurements.

List of final noise tests

Test	Figure	Commentary
Pseudo-differential single conversion vs continuous	Figure B.34	The results are close and also clearly better than prototype (Figure B.18)

List of final noise tests

Test	Figure	Commentary
Differential single conversion vs continuous, internal reference vs external	Figure B.35	The single conversion is spoiled by the fact that it took $\sim$100 conversions to stabilize. Unlikely that it has something to do with the mode, but rather with the fact it was the first test to run, which might be a problem with the settling time. Otherwise internal and external references showed identical performance, still superior to the prototype(Figure B.22)
Pseudo-differential single conversion vs continuous, 5 SPS	Figure B.36	Both test show clear reduction of noise by factor 1.5-2, and up to 1 bit better resolution
Differential single conversion vs continuous, internal reference vs external, 5 SPS	Figure B.37	

The ADC shows excellent low noise and high resolution performance. This also suggests successful PCB design, otherwise such performance would not be possible

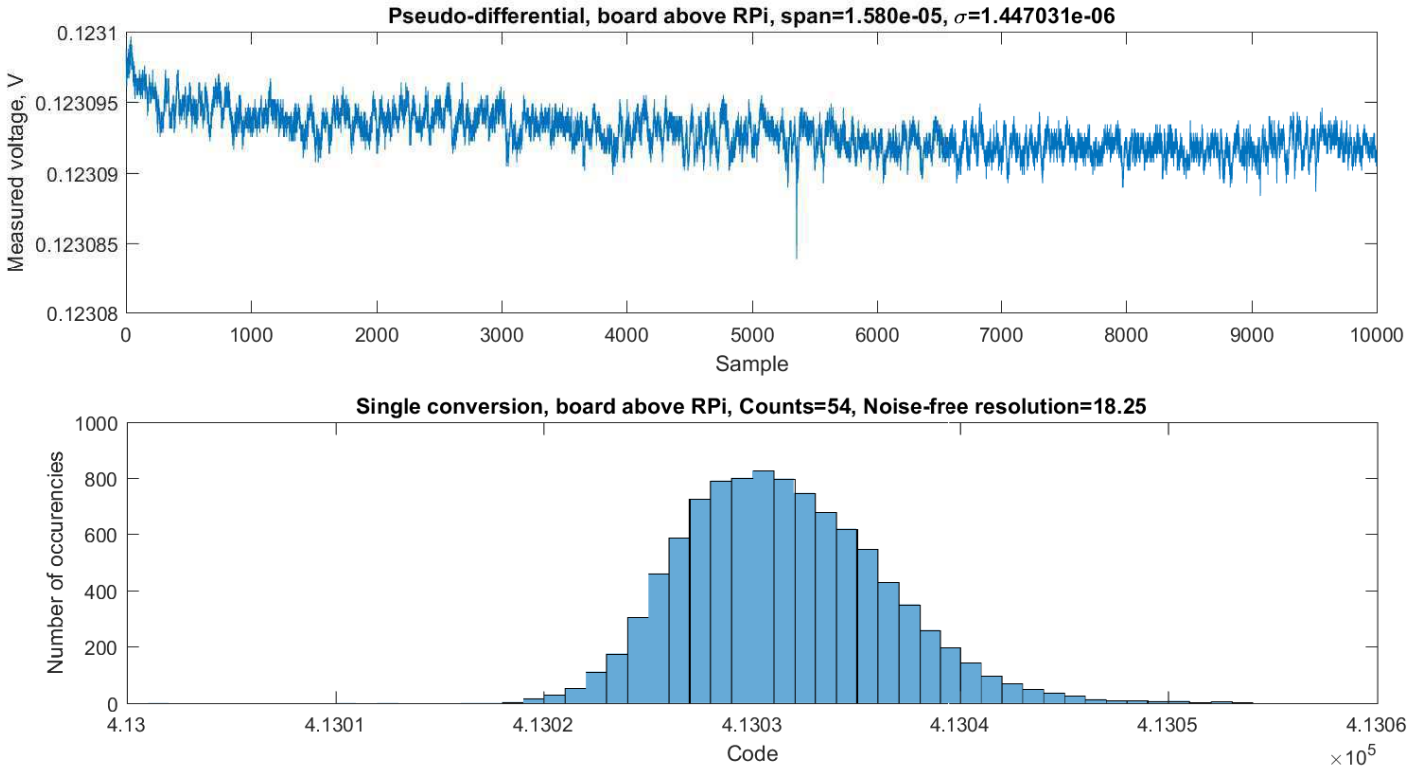

Figure B.32.: Pseudo-differential measurement, the board is above Raspberry Pi

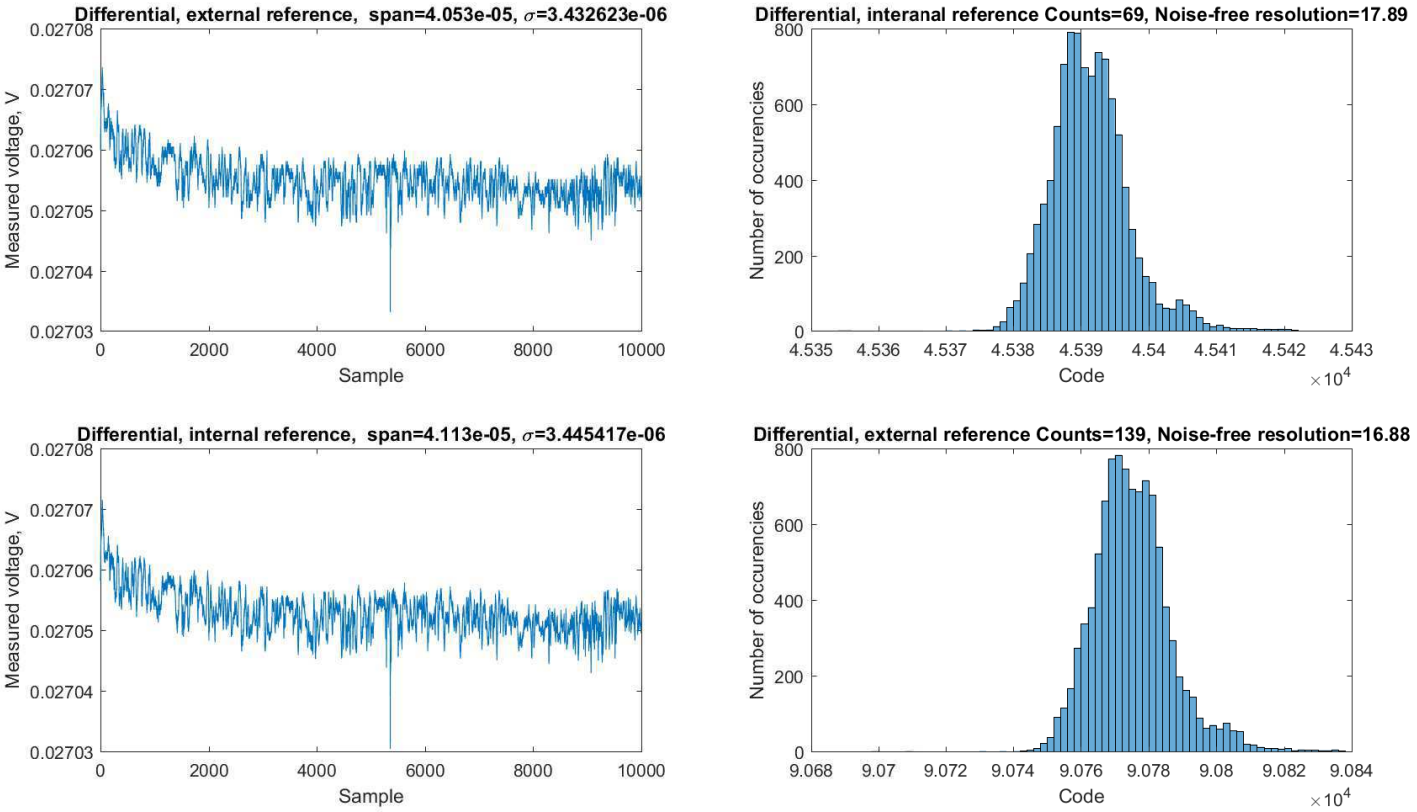

Figure B.33.: Differential measurement, the board is above Raspberry Pi

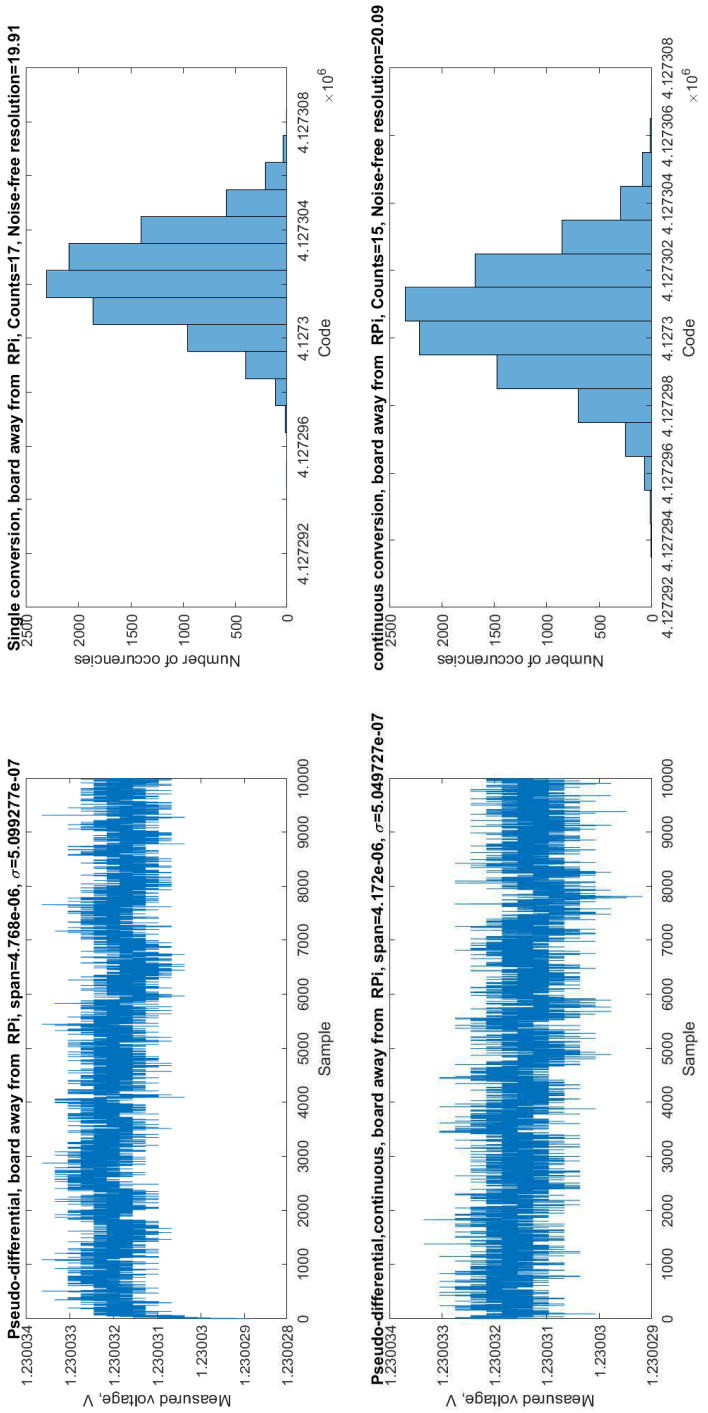

Figure B.34.: Pseudo-differential measurement, the board is away Raspberry Pi

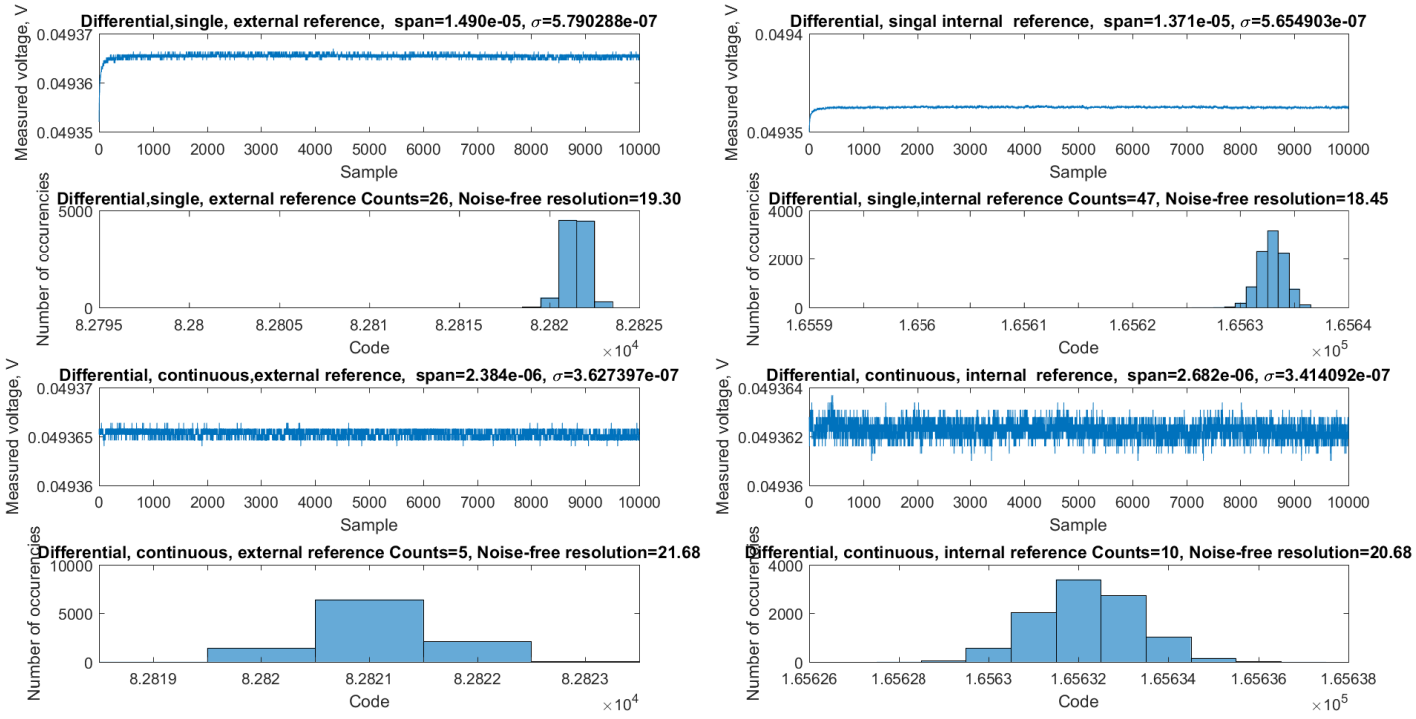

Figure B.35.: Differential measurement, the board is away from Raspberry Pi. Note, that internal reference is 2.5 V, while external 5 V. Therefore LSB with the internal reference is half of the external.

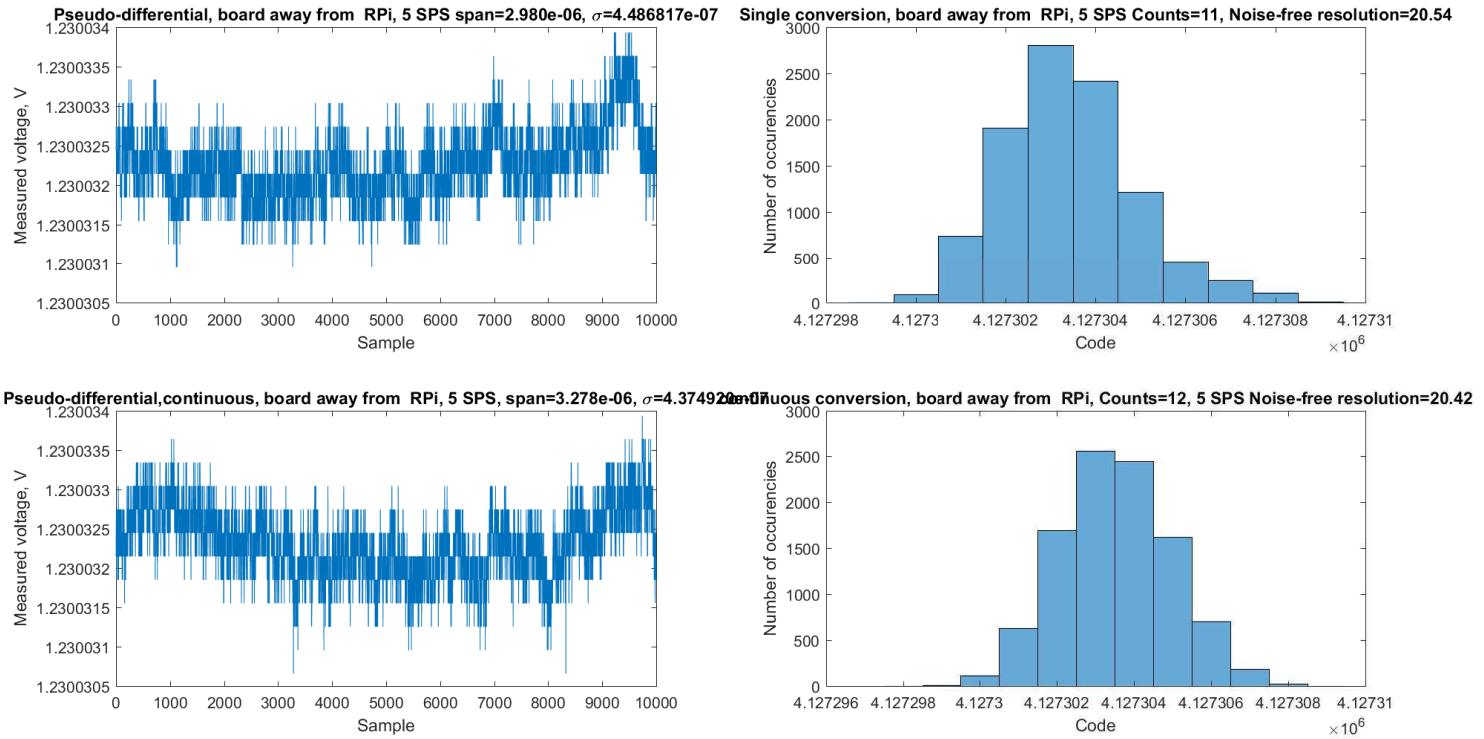

Figure B.36.: Pseudo-differential measurement, 5 SPS, the board is away Raspberry Pi

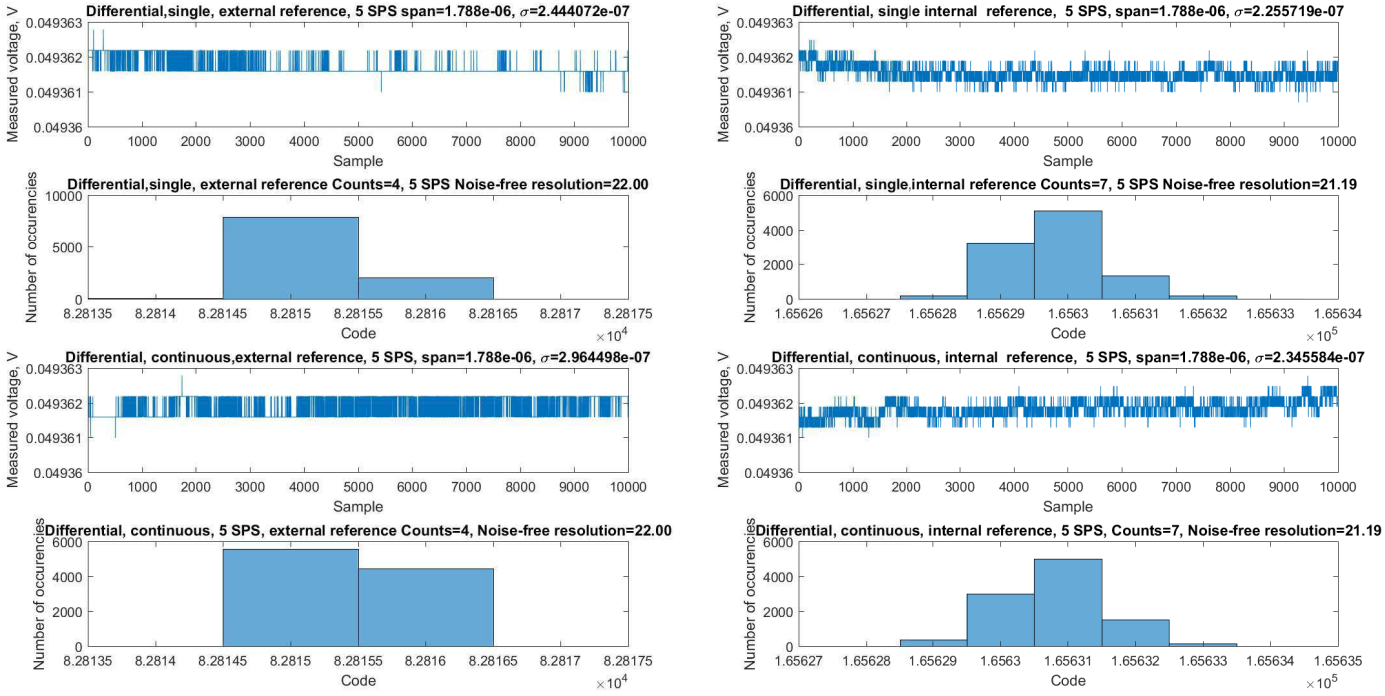

Figure B.37.: Differential measurement, 5 SPS, the board is away from Raspberry Pi. Note, that internal reference is 2.5 V, while external 5 V. Therefore LSB with the internal reference is half of the external.

B.3.2.2. Battery Tests

The tests with the batteries aim to investigate noise under conditions close to real world application. The impact of shielded cables is to be looked into. Alos a case, where cable shielding is interrupted and shield is connected together through a connector is also investigated. All tests were done using ca 1.5 m cables.

The first type of test is measuring battery voltage without charging and discharging. However, the bias currents of the ADC were enough to charge the battery making impossible direct determination of noise properties. This was overcome by fitting curve (second degree polynomial worked the best). The residuals from fitting is then the noise.

The second type is charging and discharging tests. They a focused on current measurement, since voltage was studiesd in the first test. Again, curve fitting (spline in this case) was used to isolate noise. External and internal references were compared.

List of accuracy tests.

Test	Figure	Commentary
Unshielded cable	B.38, B.39, B.40	Large low frequency interference, probably from power lines, is obvious in all measurements.
Shielded cable	B.41, B.42, B.43	The interference is completely disappeared. The noise is only slightly larger than in Figure B.34, Figure B.35
Shielded cable, shield through connector	B.44, B.45, B.46	The interference reappears, although still much lower than unshilded.

The cable shielding really proved itself and is highly recommendable. The difference between internal and external referncec is marginal, so either could be used.

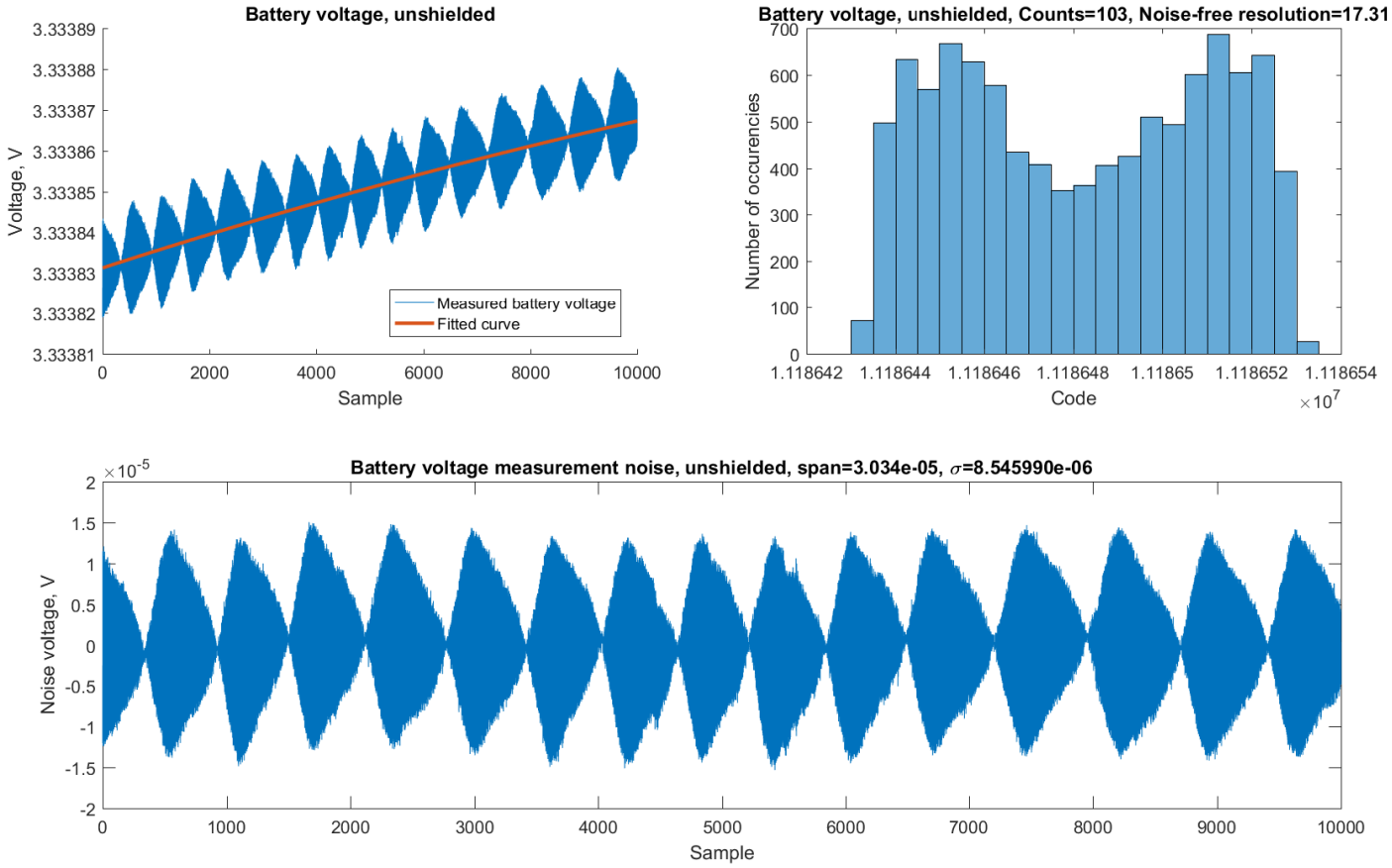

Figure B.38.: Battery voltage measured with an unshielded cable

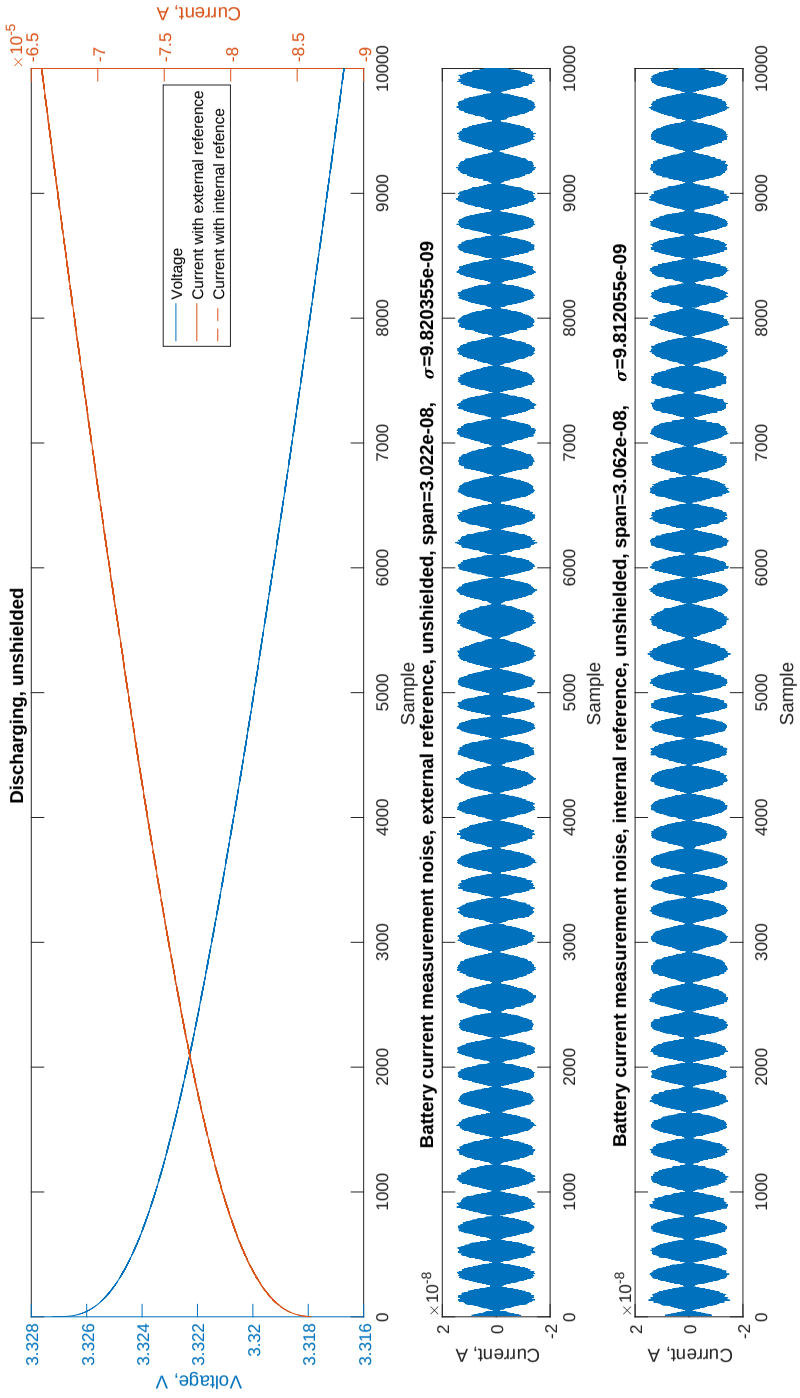

Figure B.39.: Battery discharging, measured with an unshielded cable

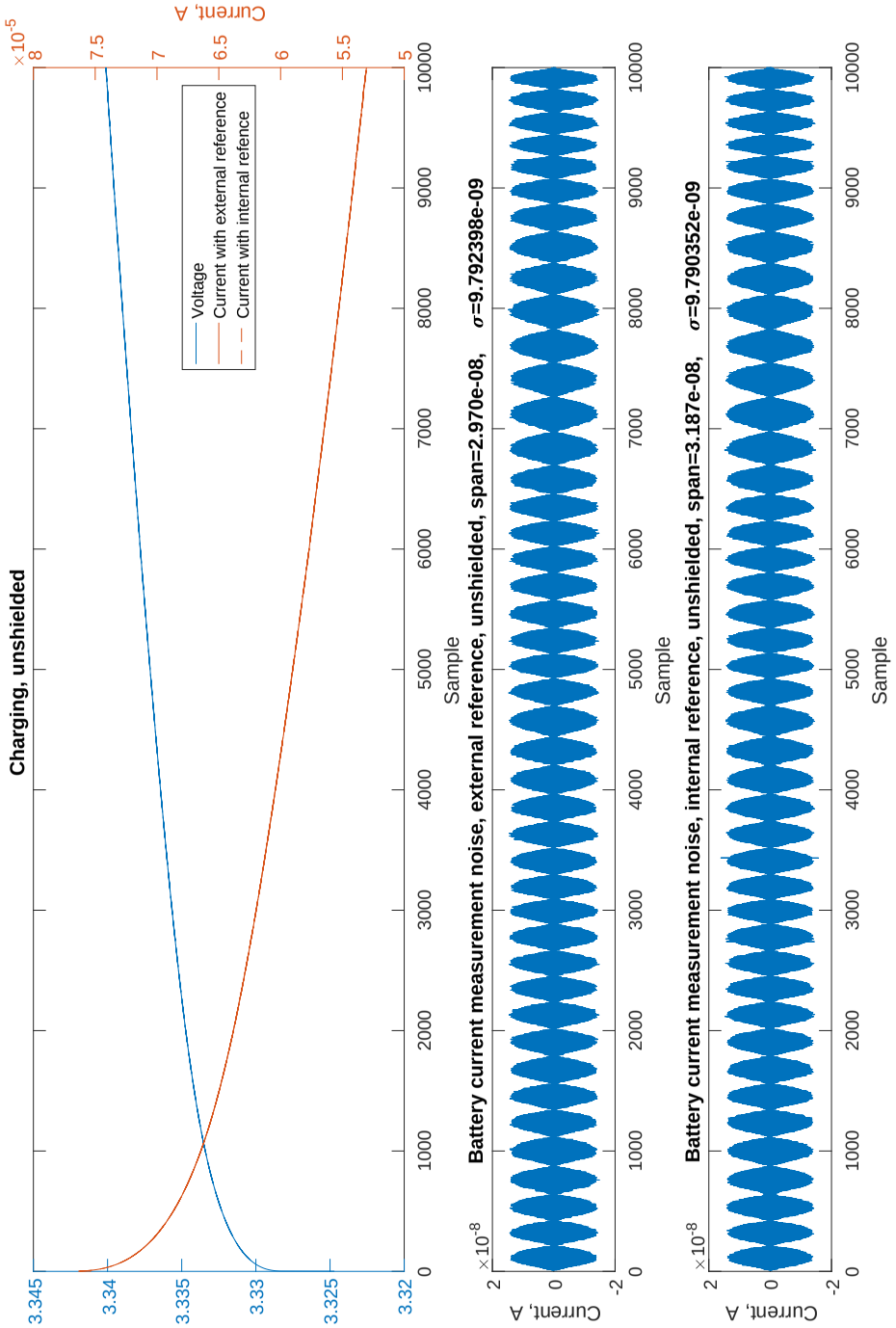

Figure B.40.: Battery charging, measured with an unshielded cable

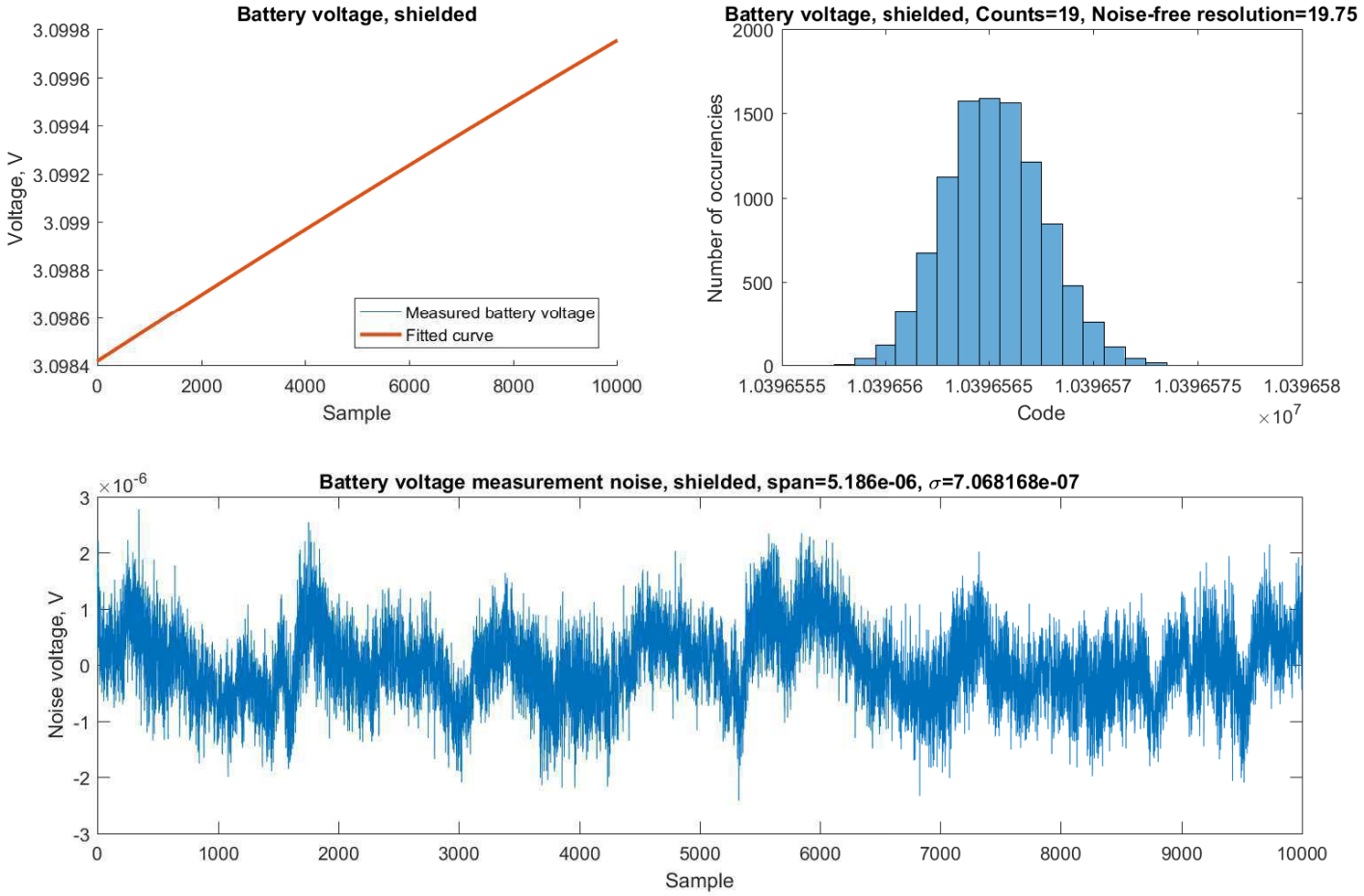

Figure B.41.: Battery voltage measured with a shielded cable

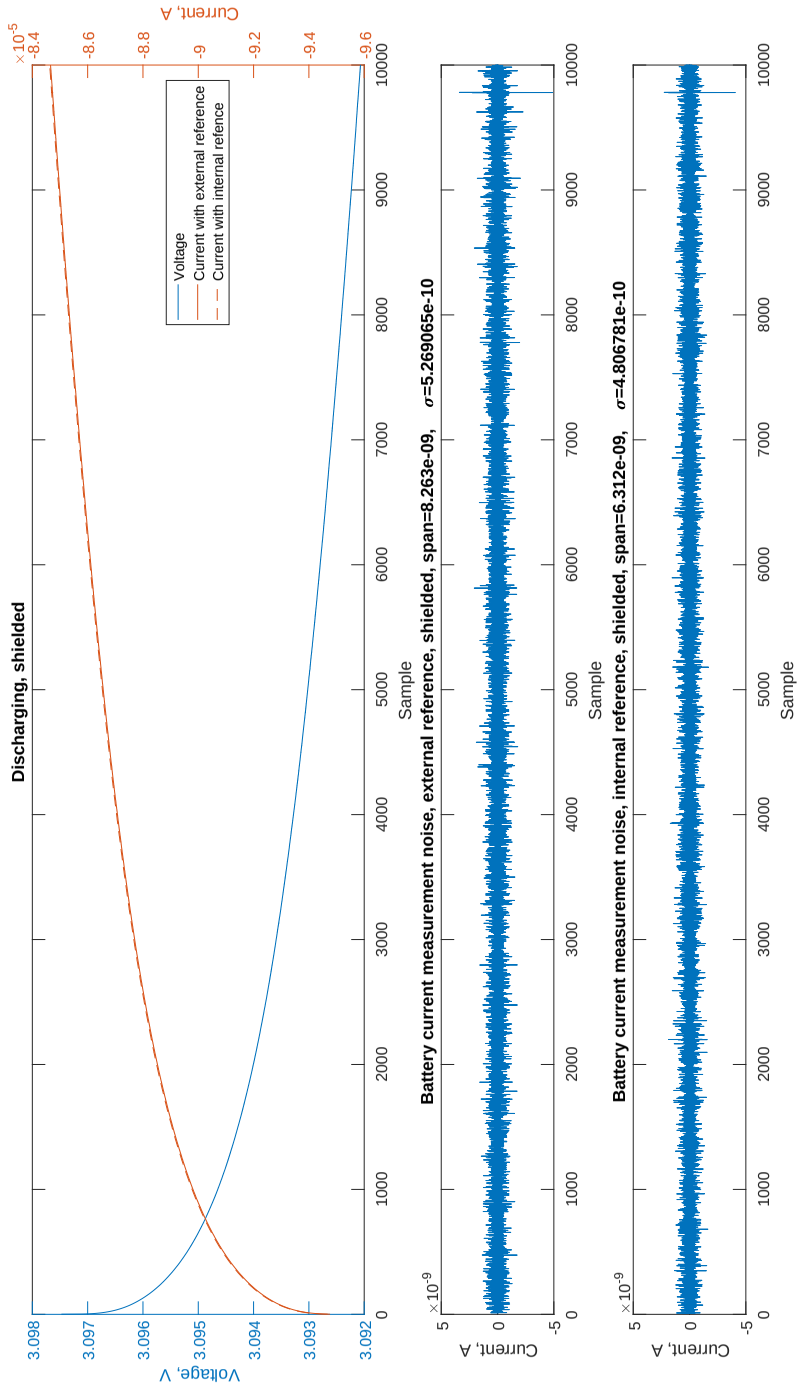

Figure B.42.: Battery discharging, measured with a shielded cable

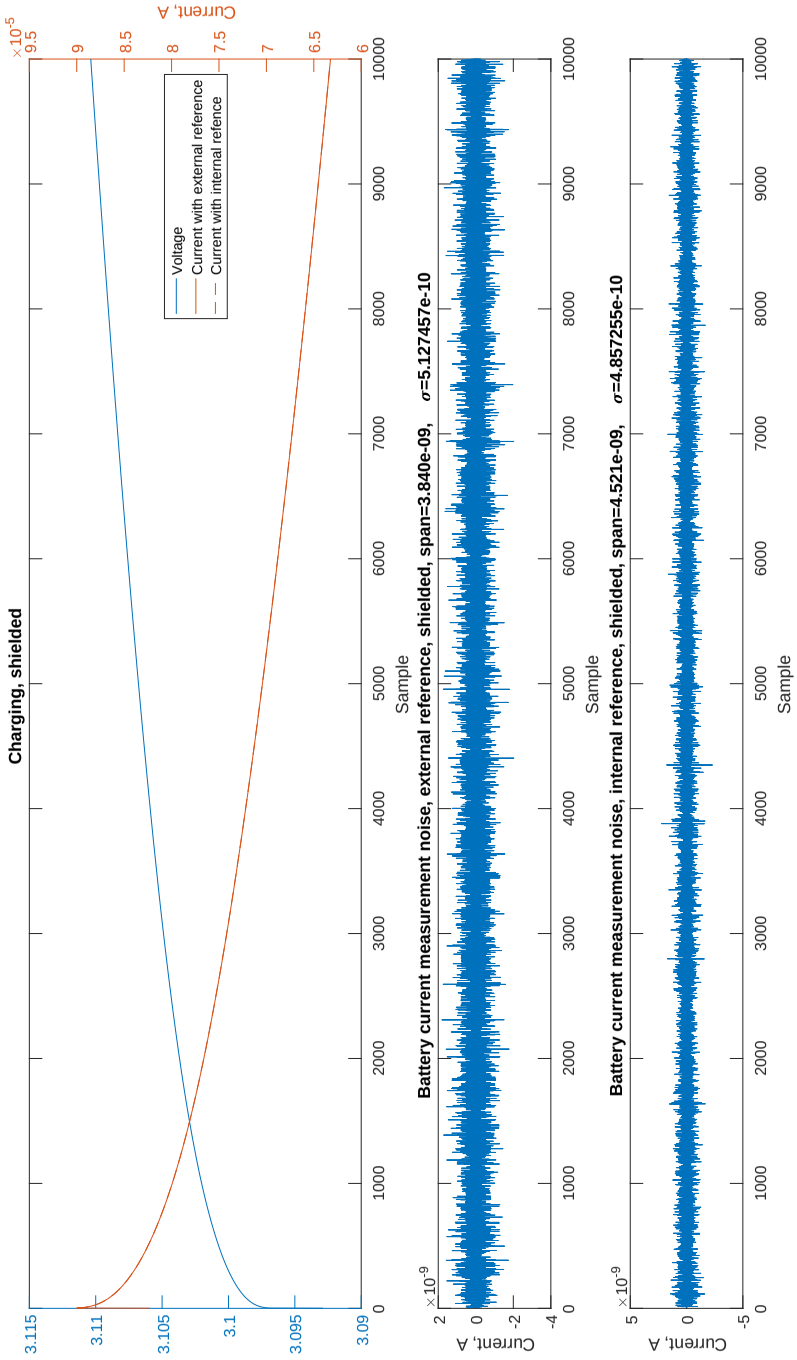

Figure B.43.: Battery charging, measured with a shielded cable

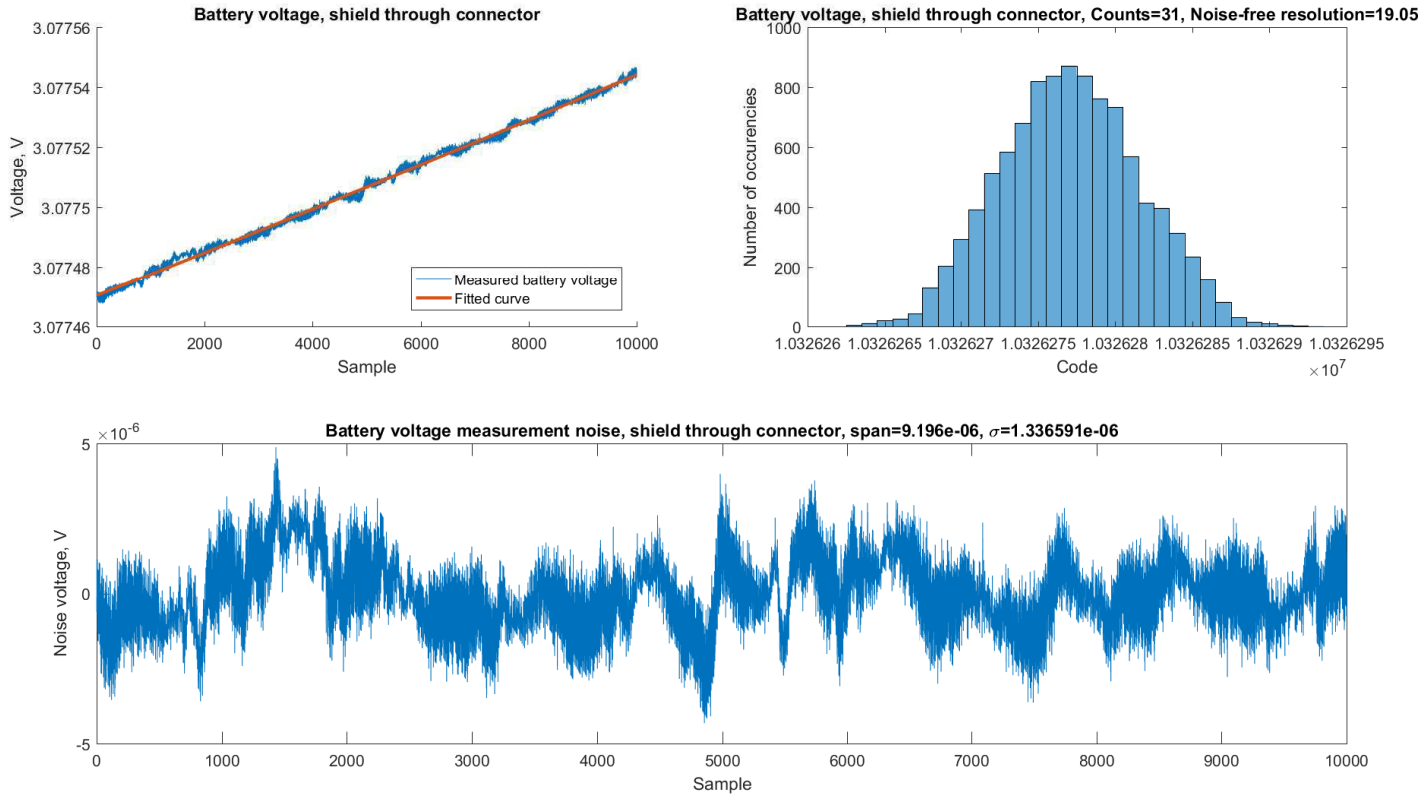

Figure B.44.: Battery voltage measured with a cable whose shielding interrupted by a connector

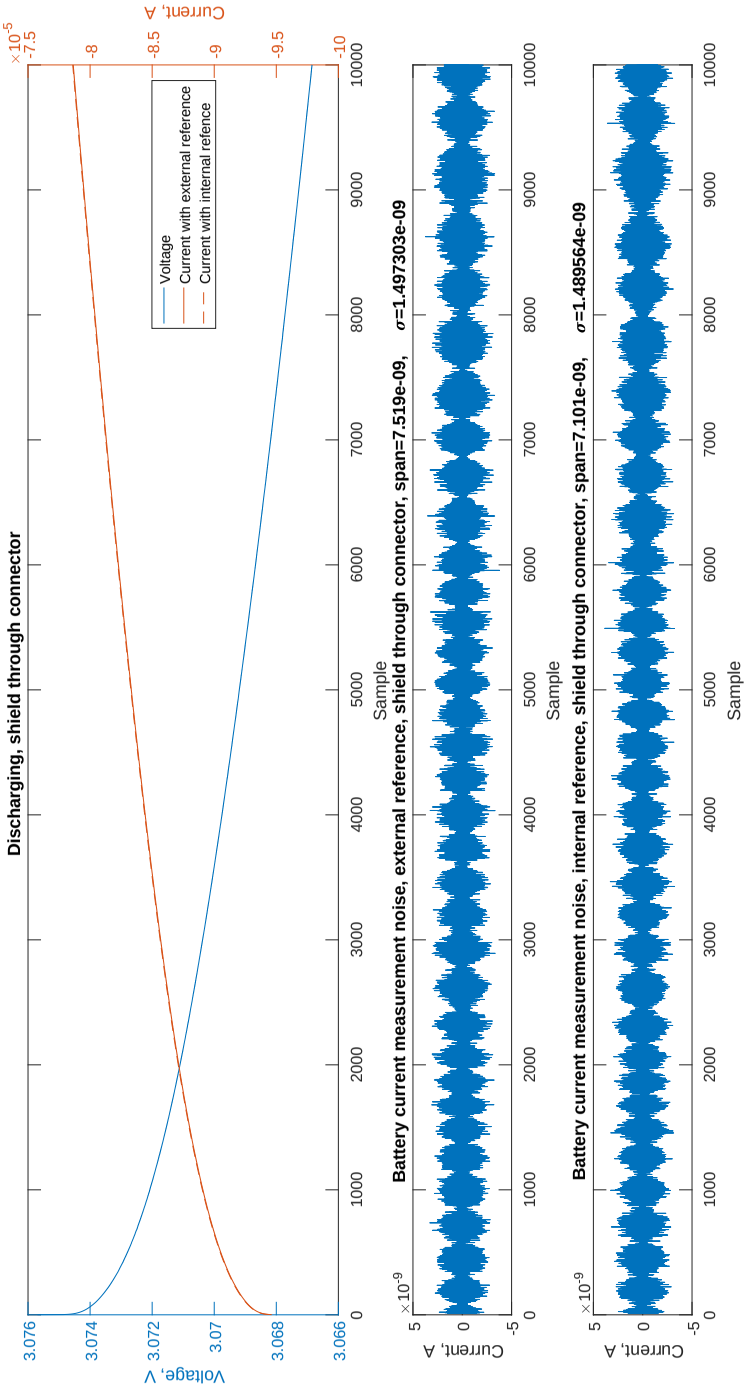

Figure B.45.: Battery discharging, measured with a cable whose shielding interrupted by a connector

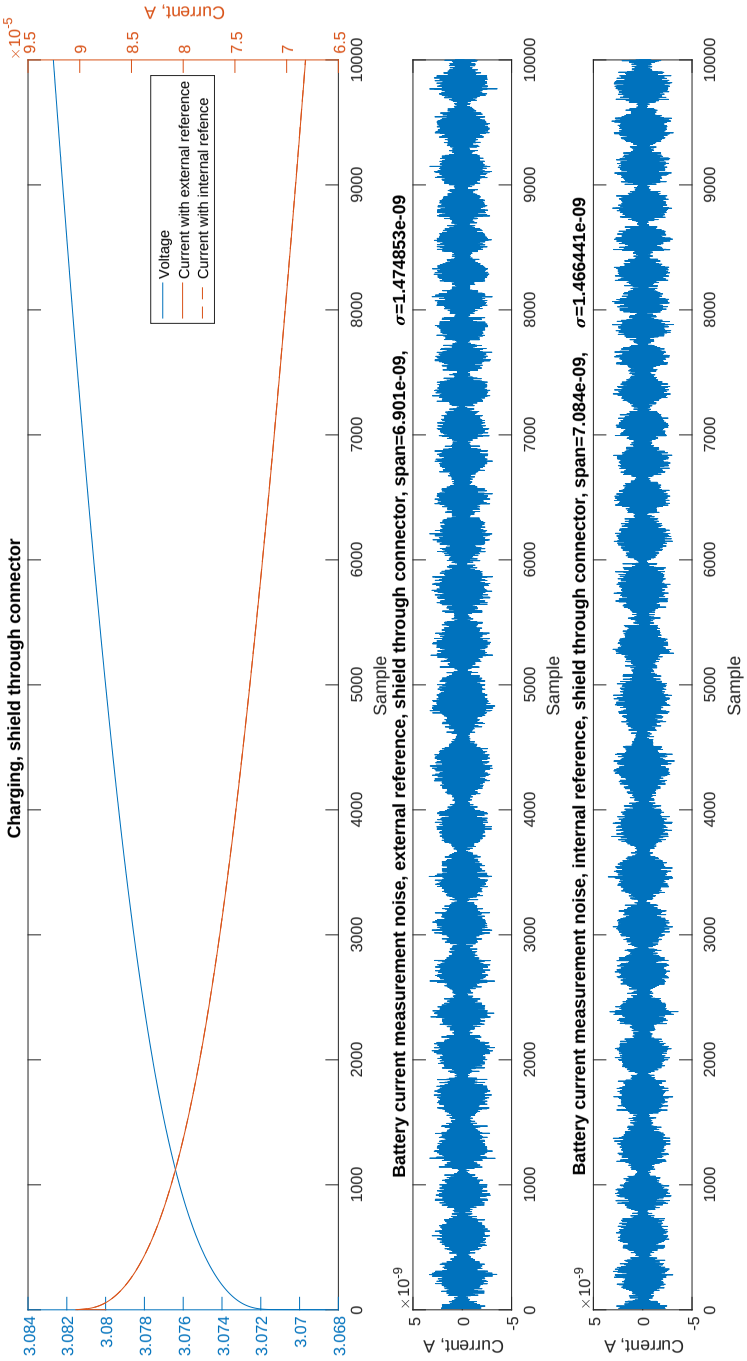

Figure B.46.: Battery charging, measured with a cable whose shielding interrupted by a connector

B.3.2.3. Accuracy Tests

The accuracy tests compare measurement of charging (Figure B.48) and discharging (Figure B.47) currents with DMM4020. Again, while looking on results one also should keep in mind that taking samples wasn't simultaneous. That is, there is a varying delay between the DMM and the ADC. The measurements were performed over unshielded cables that explains the relatively large apparent oscillations. The ADC channels were offset calibrated.

The charts show satisfying results with acurracy around 50 nA.

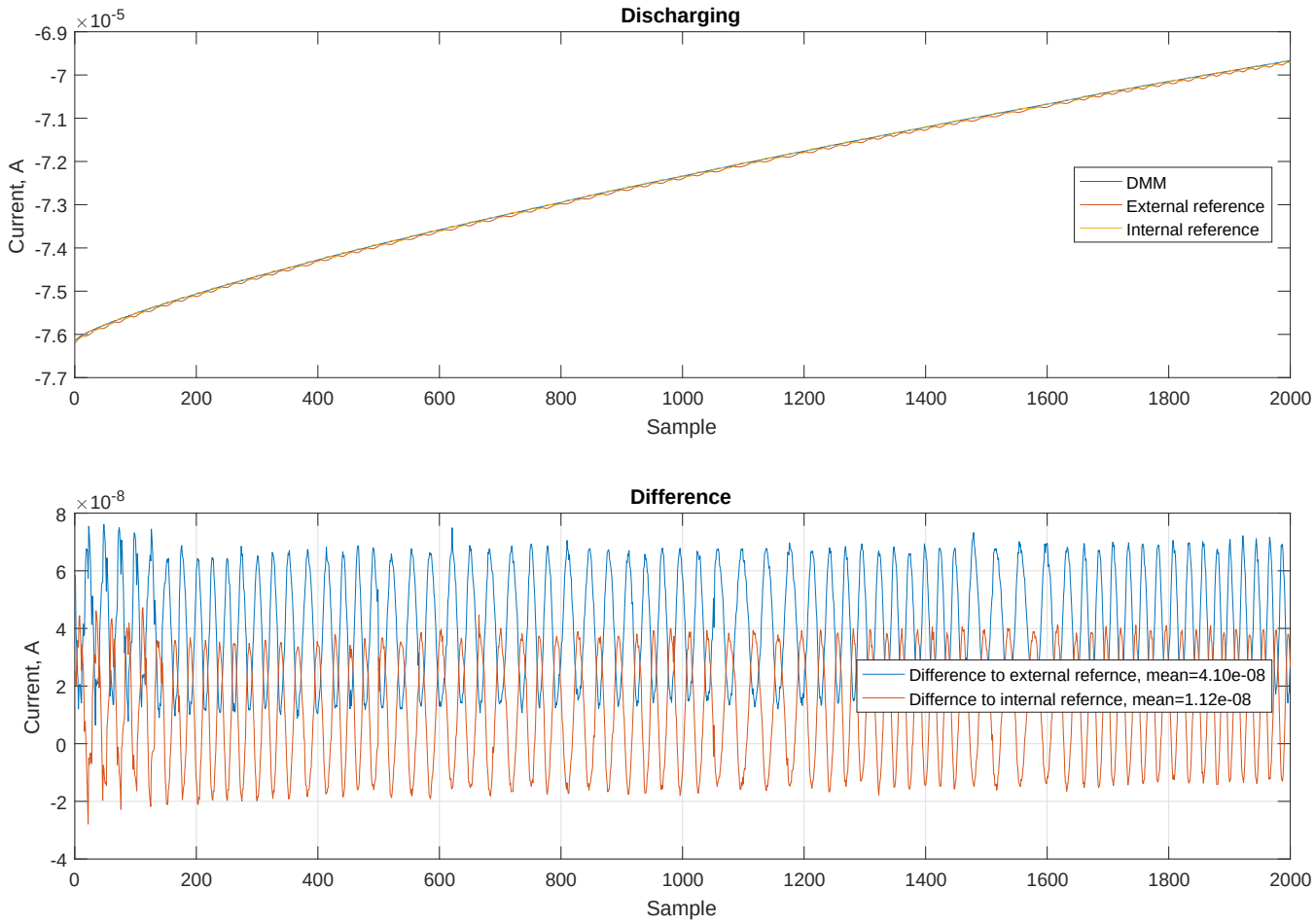

Figure B.47.: Discharging in comparison with DMM4020

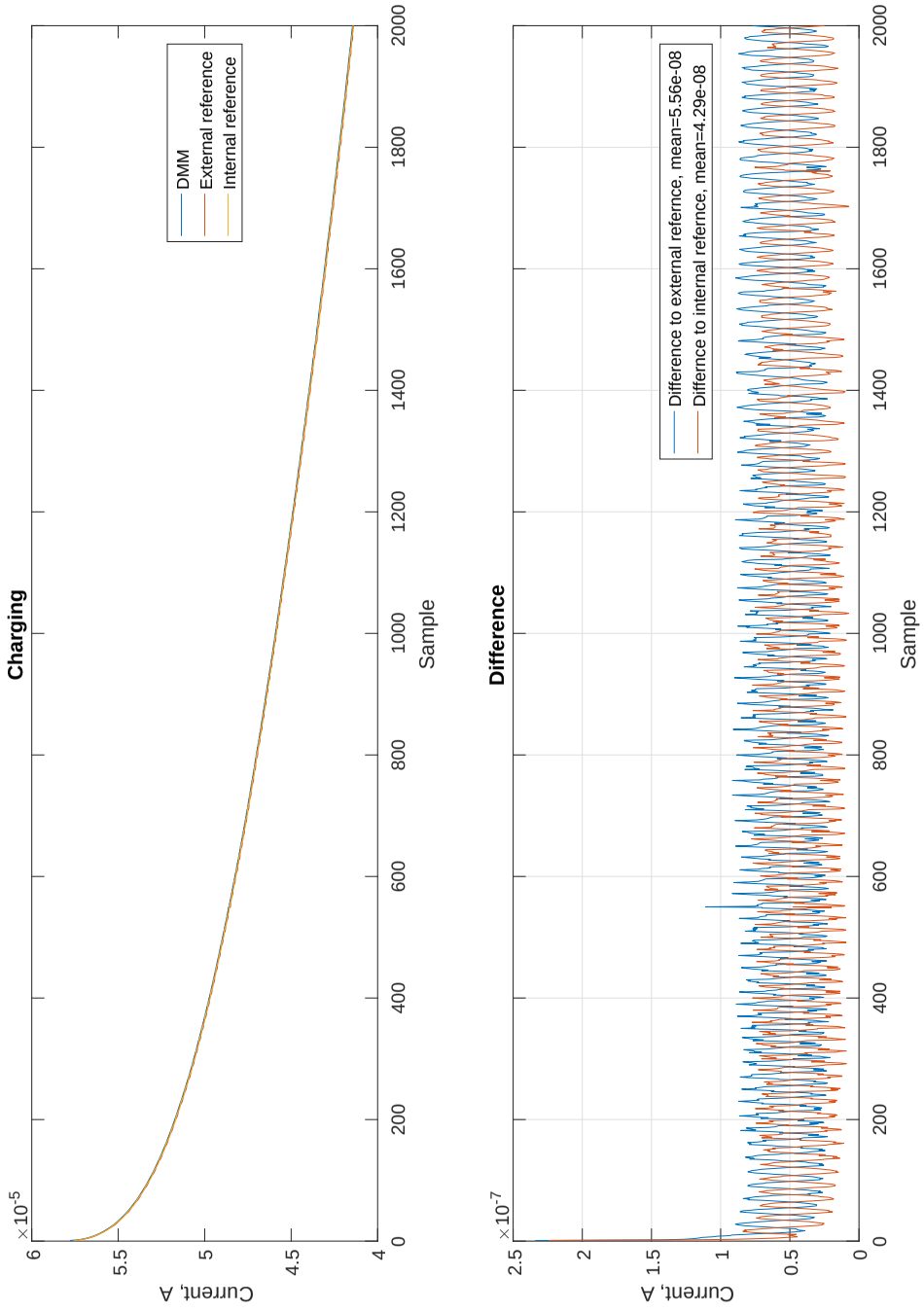

Figure B.48.: Charging in comparison with DMM4020

B.4. LED Control

The test circuit was assembled on a RE 435LF prototyping board (Figure B.49). The pitch of the board is larger than TSSOP package of the AD5684R that is why the DAC was mounted on an adapter board. The power supply was provided by AD7118 LDO, while the 3.3 V for digital interface was sourced from the Raspberry Pi. The verification of correctness of the electrical circuit was performed with an ohmmeter.

To simplify the testing a graphical application *LEDControlDemo* was build with Qt (a GUI framework) (Figure B.50). The application is capable assigning colour channel to any DAC output. The brightness of LEDs could be successfully controlled with it. However, the LEDs noticeably flickered at certain brightness levels and the LED drivers were heated up. The designer of the driver circuit S. Pereguda was consulted and he suspected peaks of the output voltages of the drivers. This was confirmed with an oscilloscope (Figure B.51). Installation of a 10 μF capacitor per designer's recommendation to smooth the output voltage resolved the problem (Figure B.52). After that the LED control module functioned exactly as supposed .

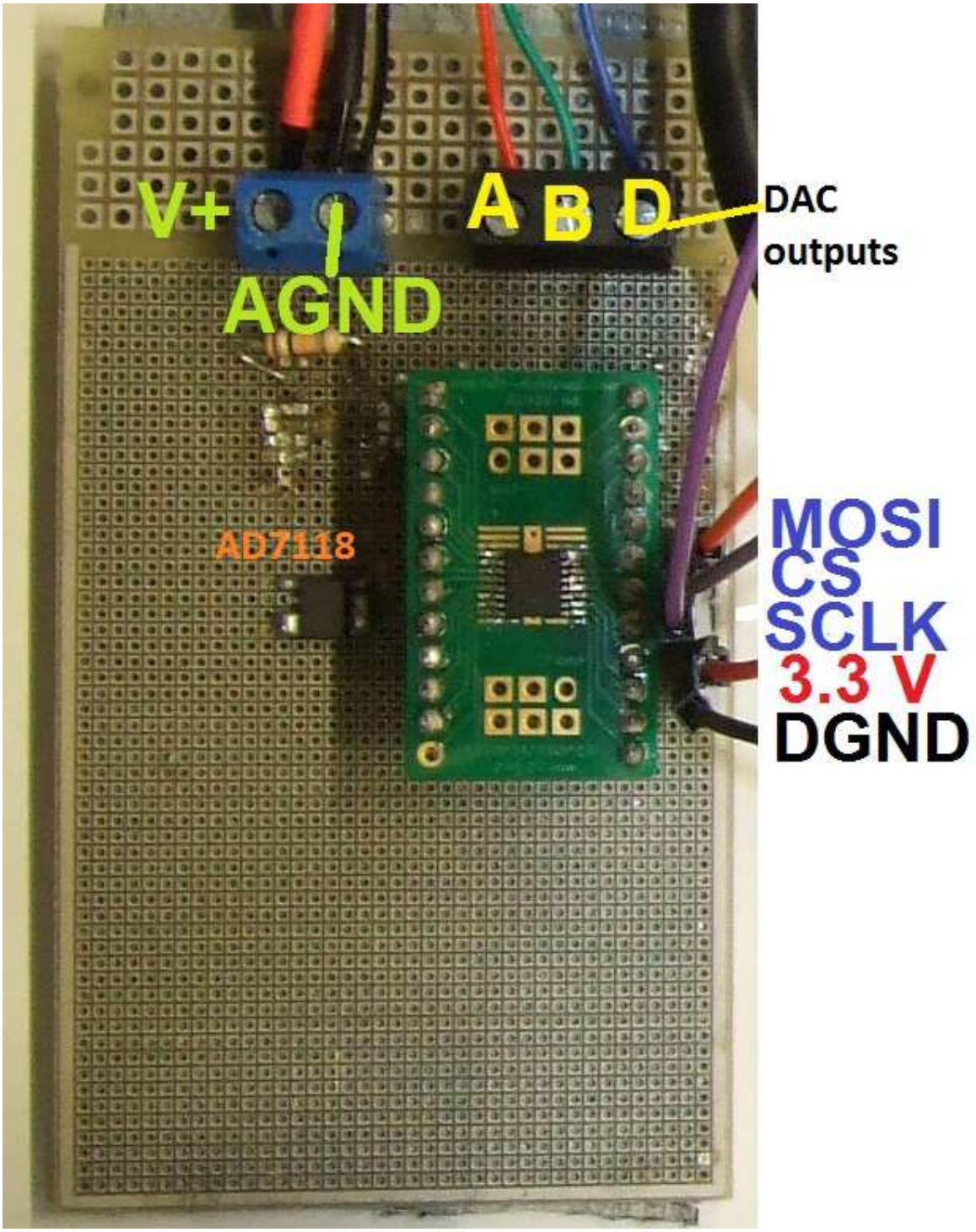

Figure B.49.: The prototype of the LED control. AD7118 was used for simpicity as it could be directly soldered to the perfboard.

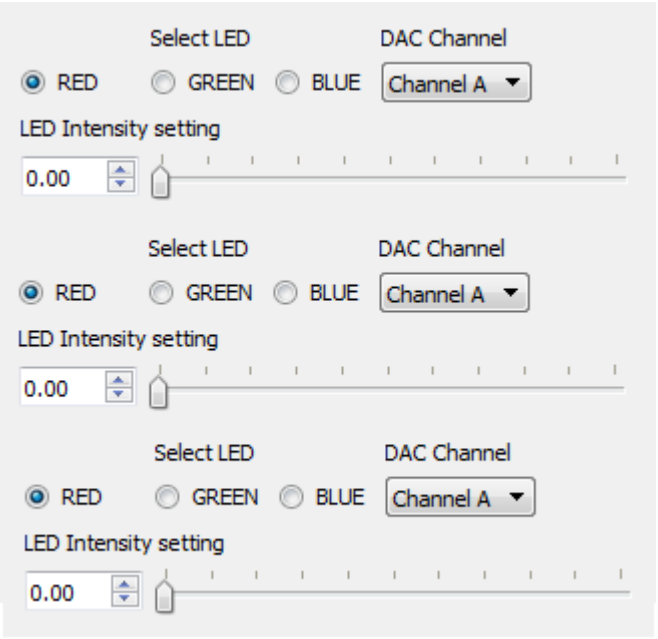

Figure B.50.: GUI of the LEDControlDemo application

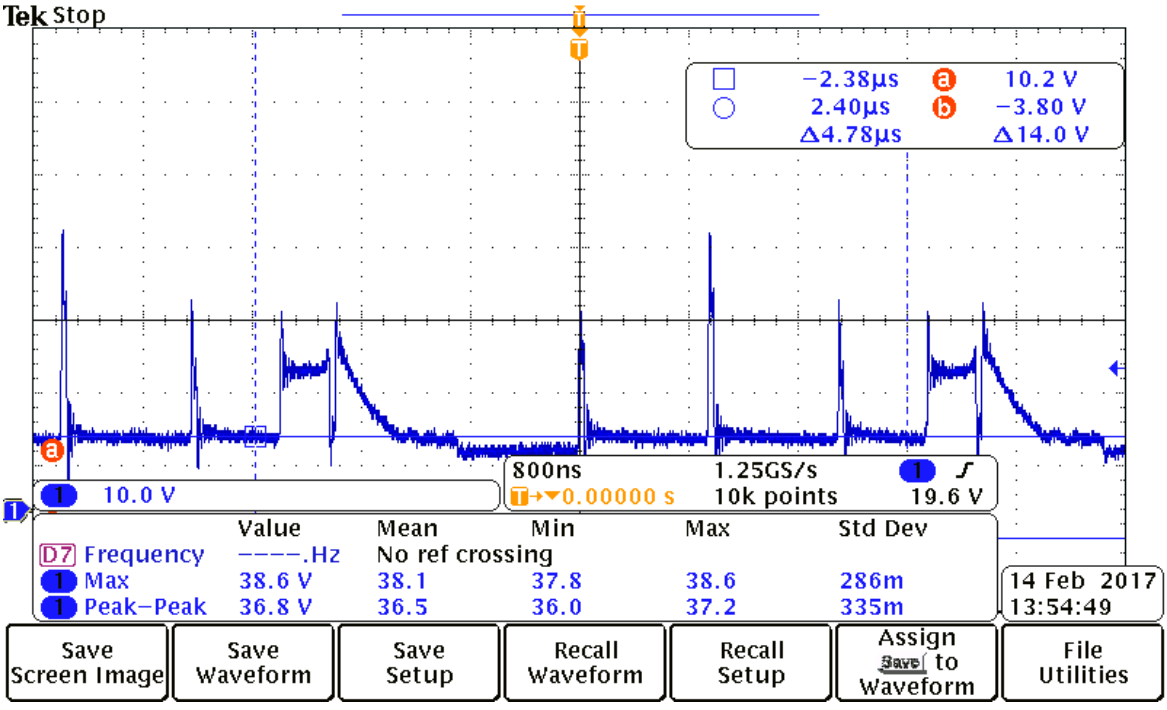

Figure B.51.: Output voltage of the red LED driver. This driver ewas heated up by peaks of the output voltage

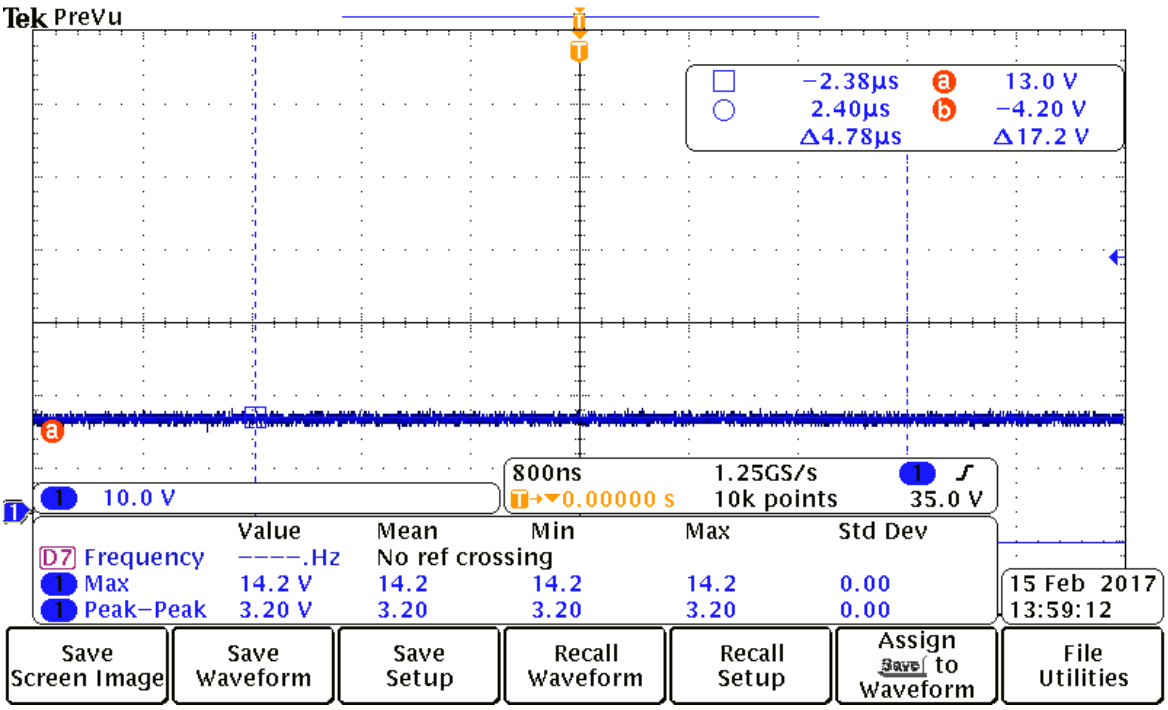

Figure B.52.: Output voltage of the red LED driver after addition of a 10 μF output capacitor. The output is now DC.

B.5. Software

This appendix contains tests specifications for the software. The most test were performed either by observing output. In many cases the digital oscilloscope was used to monitor the SPI transactions and verify their correctness.

B.5.1. Basic Functions

Table B.9.: Test specifications for basic communication on Raspberry Pi

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status or Proof**
GPIO output logic state	`GPIOPin::setState()`	An LED is connected to GPIO pin. The pin must blink.	pass
GPIO pullup and pulldown	`GPIOPin::setPullMode()`	The GPIO pin can be set into pull up and pull down eith internal resistors.	pass
GPIO input test	`GPIOPin::getState()`	The pin is in the input mode and pulled to “low”. Every time it shorted to 3.3 V (voltage level of “high”), a string is printed in the console.	pass
GPIO input event	`GPIOPin::setEvent()`, `GPIOPin::waitForEvent()`	A button is connected to a GPIO pin on while the event is set to rising edge. Every time the button is pressed, a string is printed in the console.	pass

Table B.9.: Test specifications for basic communication on Raspberry Pi

Test case	Relevant functions	Method of testing and expected output or behaviour	Status or Proof
SPI transmit and readback	`SPI::transmit()`	MISO and MOSI are connected. All 8-bit values are sent over and read back with SPI. The read back values are shown in the console	pass

B.5.2. ChipSelect, SPIDevice

For this test protected and private member functions were temporary made public.

Table B.10.: Test specifications for basic communication on Raspberry Pi

Test case	Relevant functions	Method of testing and expected output or behaviour	Status

Full SPI transaction of 1 byte	`SPIDevice::transferInt<char>()`
	`ChipSelect::activate()`
	`ChipSelect::deactivate()`
		Byte value 75 is sent over SPI and read back. Chip select is activated and deactivated appropriately.	pass: Figure B.53

Full SPI transaction of an integer	`SPIDevice::transferInt<int>()`
	`ChipSelect::activate()`
	`ChipSelect::deactivate()`
		Integer value 0x1c47de2a is sent over SPI and read back. The bytes are transmitted in correct order. Chip select is activated and deactivated appropriately.	pass: Figure B.54

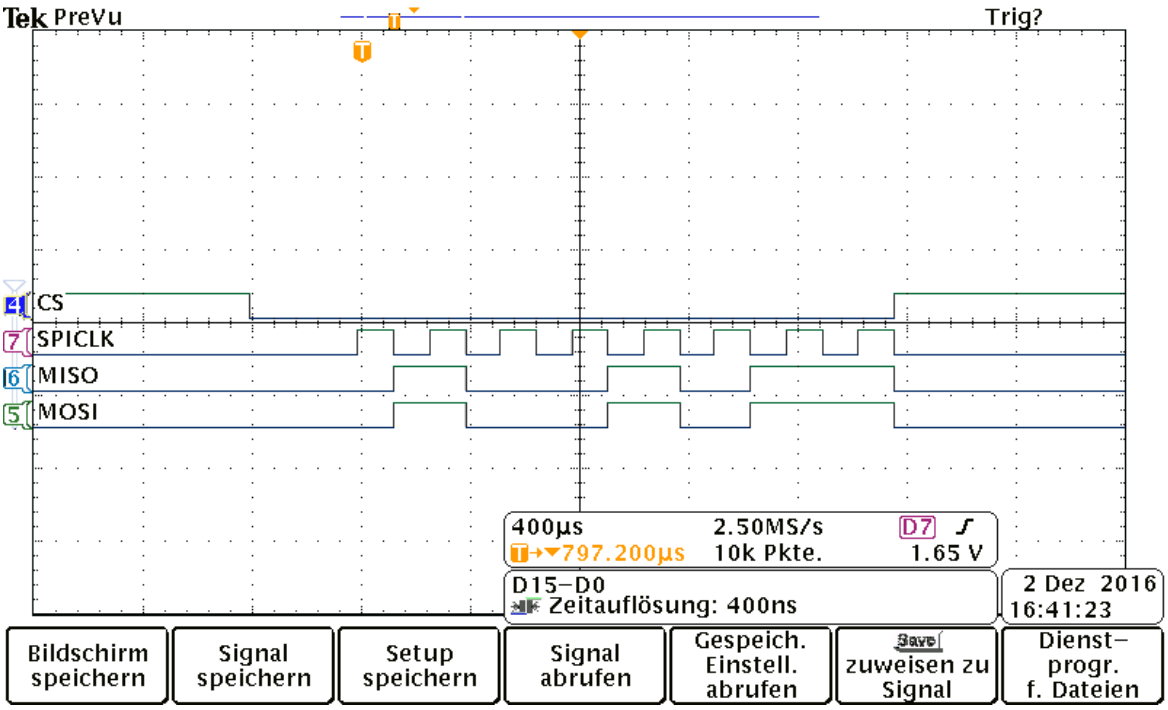

Figure B.53.: Digital oscilloscope image of transaction 1 byte value 75. Chip select is properly activated deactivated

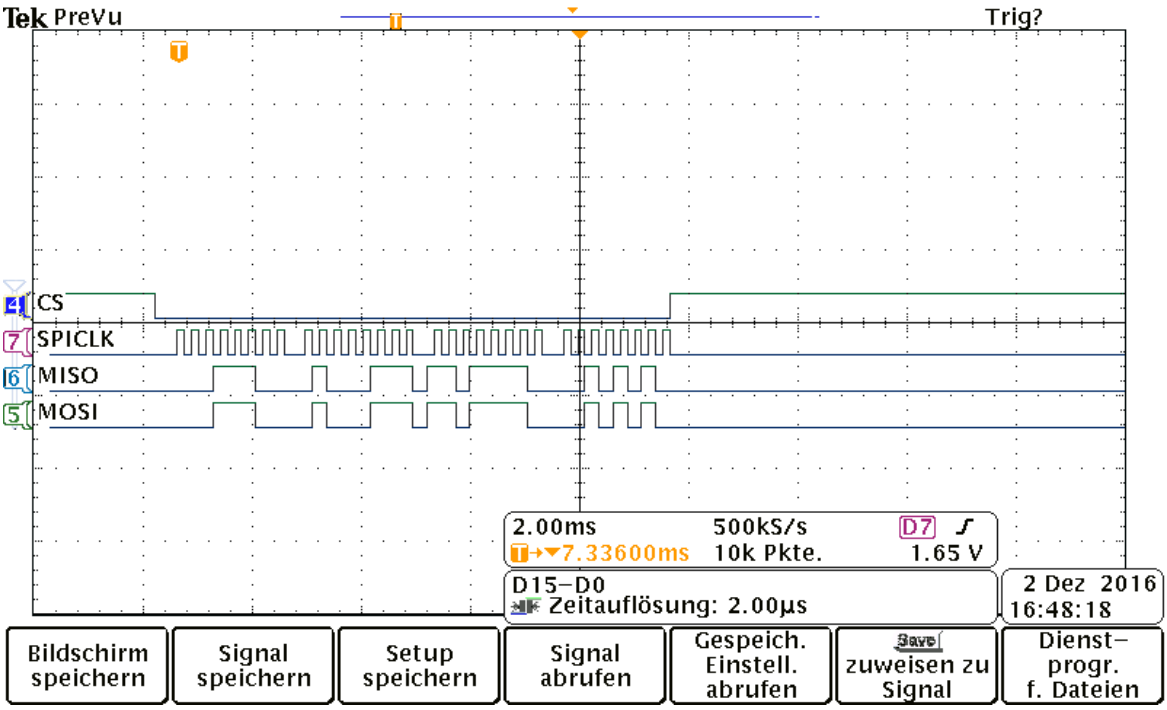

Figure B.54.: Digital oscilloscope image of transaction of int value 0x1c47de2a. Chip select is properly activated deactivated

B.5.3. Common Functions of Data Converters

Table B.11.: Test specifications for basic functions of data converters

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
Setting up a channel	`ADC::setChannel()`	The function corectly sets and computes channel parameter. Verified with the debugger.	Pass
Conversion to real quantity	`ADC::convertToReal()`	The function applies channel parameters and converts the code to the real quantity	Pass
Conversion to code	`DAC::convertToCode()`	The function applies channel parameters and correctly converts real quantities to codes	pass

B.5.4. AD5684R and LED Control

Table B.12.: Test specifications for AD5684R and LED Control

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
Enable channel	`AD5684R::enableChannel`	A channel gets enabled	pass
Input register	`AD5684R::writeInput()`	Input register can be written with value.	pass
Update DAC	`AD5684R::updateDAC()`	The DAC gets updated with the value in the input register	Pass
Set DAC output	`AD5684R::write()`	The output voltage of a channel is set to commanded value.	pass

Table B.12.: Test specifications for AD5684R and LED Control

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
disable channel	`AD5684R::disableChannel()`	A channel becomes disabled	pass
Assign a LED to an output channel	`LEDControl::assignColorChannel()`	A LED (red, green or bluer) is assigned to a the output of the AD5684R	pass
Set LED intensity	`LEDControl::setColourChannel()`	The LED intensity is changed to commanded intensity in percentage.	pass

B.5.5. MAX5318

Table B.13.: Test specifications for MAX5318 DAC

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
Reset	`Max5318::reset()`	All registers are cleared and reset to default values	pass
Enable device	`Max5318::enableChannel()`	The DAC is enabled and outputs default value	pass
Function of Busy pin	`Max5318::enableBusyInput()`	The function busys pin can be set	pass
Set output of the DAC	`MAX5318::write()`	The DAC output is changed to correct commanded voltag	pass
Set offset	`Max5318::setOffset`	The offset register is written with offset vale. The output of the DAC adjusts itself accordingly	pass

Table B.13.: Test specifications for MAX5318 DAC

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
Set gain	`Max5318::setGain`	The gain register is written with gain value. The output of the DAC adjusts itself accordingly	pass
enable read back	`Max5318::enableOutput()`	The read back becomes enabled	pass
read offset	`Max5318::getOffset()`	The offset configuration is read back and compared to the previously set value	pass
read gain	`Max5318::getGain()`	The gain configuration is read back and compared to the previously set value	pass
Get configuration	`Max5318::getConfig()`	The content of configuration register can be read from the DAC	pass
Revision	`Max5318::getRevision()`	The revision of the device can be read	pass

B.5.6. AD7175-2

Table B.14.: Test specifications for AD7175-2 ADC

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
ID read	`AD7175_2::test()`	The ID (0x0CDX)of the ADC can be read for the purpose of testing communication	pass
Enable channel	`AD7175_2::enableChannel()`	A channel becomes enabled, whereas multiple channel can be enabled	pass

Table B.14.: Test specifications for AD7175-2 ADC

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
Channel setup	`AD7175_2::setup()`	The bipolar mode can be, set, input and reference buffers enabled and the source of reference voltage selected	pass
Filter order selection	`AD7175_2::setFilterOrder()`	The filter order can be selected	pass
Input assignment	`AD7175_2::assignInputToChannel()`	The analog inputs can be successfully assigned to a channel	pass
Data rate	`AD7175_2::setDataRate()`	Output dta rate cna bee successfully changed	pass
ADC mode	`AD7175_2::setADC()`	The internak refernce and single cycle settling can be enable or disable. TH ADC successfully converts in both single and continuous conversion modes.	pass
Get values from ADC	`AD7175_2::waitForUpdate()`	The function waits for all active channels to complete conversion. It retrieves result codes from and stores them locally.	pass
Real value	`ADC::read()`	Th function gets the conversion result as code and returns it as a real word quantity	pass

B.5.7. Multimeter

Table B.15.: Test specifications for digital multimeter

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
function selection	`Multimeter:: setFunction()`	Measurement function on both primary and secondary display can be selected	pass
Trigger mode	`Multimeter:: setTriggerMode()`	The trigger mode can be successfully selected	pass
Retrieve measurement	`Multimeter:: waitForUpdate()`	The function successfully retrieves measurement results from both displays and stores them locally.	pass

B.5.8. DataLogger

Table B.16.: Test specifications for DataLogger class

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
Folder setting	`DataLogger::setFolder`	The folder is set and created if doesn't exist	pass
output file	`DataLogger::setFile()`	The output file is created.	pass
Column titles	`DataLogger:addColumns()`	The titles of columns are stored	Pass
column output	`DataLogger:: writeColumns()`	The column headers are written to the file	pass

Table B.16.: Test specifications for DataLogger class

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
logging data	`Datalogger::log`	A row of data is written to the file. The function must accept arbitrary number and types of arguments.	Pass

B.5.9. Relay

The state of the relay was checked by probing the contacts with Ohmmeter.

Table B.17.: Test specifications for Relay

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
close relay	`Relay::close()`	The relay closes	pass
open relay	`Relay::open()`	The relay opens	pass
toggle relay	`Relay::toggle()`	The state of relay alternates	pass

B.5.10. Real Time Clock

Table B.18.: Test specifications for DS3432 RTC

Test case	Relevant functions	Method of testing and expected output or behaviour	Status
setting system time	`RTC:: setSystemTimeFromRTC()`	The system time can be set from the RTC	pass
set RTC	`RTC:: setRTCFromSystemTime()`	RTC can be updated with system time	pass
set time	`DS3234::writeTime`	The time is successfully written to the RTC	pass

Table B.18.: Test specifications for DS3432 RTC

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
retrieve day of week	`DS3234::getDayOfWeek`	Day of week can be obtained from the DS3432	pass
retrieve date	`DS3234::getDate()`	The date can ve retrieved fom the RTC	pass
retrieve time	`DS3234::getTime()`	The time can be retreived from the RTC	pass
Get temperature	`DS3234::getTemperature()`	The internal sensor is read and the temperature is returned	pass
AM/PM	`DS3234::getAMPM()`	The correct half of the day is returned	pass
Time format	`DS3234::writeTimeFormat()`	The time format is set and representation is adjusted	Failed: the conversion between time formats doesn't work reliably

B.5.11. Implementation Selection

Table B.19.: The possibility of selecting the controlling of digital interface either directly over the registers or over the operating system and os implementation are tested

Test case	**Relevant functions**	**Method of testing and expected output or behaviour**	**Status**
implemnatation selection	`setImpl()`	The implementation of the library (registers/OS) is selected	pass
OS implemetation	The tests listed in Sections B.5.1 and B.5.2 repeated for OS/driver implementation. So are most important tests for component classes		pass

Appendix C.

Clamps, Pin Connectors and Test Points

This appendix documents the purpose and function of all external connectors on the PCB.

Table C.1.: Test Points on the the PCB. The test points serve verification and debugging of the board.

Test point	**Function**
TP1	5.49 V power supply
TP2	5 V reference
JP2	Output voltage of the MAX5318 DAC. Implemented as pin to allow fixed connection.

Table C.2.: POWER clamp connects to the external PSU

Pin	**Function**
9V	9 V external voltage supply
GND	external ground

Table C.3.: CHARGE_OUT clamp provides charging and discharging currents to the battery

Pin	**Function**
Iout	should be connected to the cathode of the battery
return	return currents from the battery
shield	for connected of the cable shield

Table C.4.: V_BAT clamp serves the voltage measurement

Pin	Function
BAT+	should be connected to the cathode of the battery
BAT-	should be connected to the anode of the battery
shield	for connected of the cable shield

The first and the last pins of the pin connectors are marked on the PCB.

Table C.5.: JP1 is the main pin connector to Raspbberry Pi

Pin on Raspberry Pi	Pin on PCB	Function		Pin on PCB	Pin on Raspberry Pi
11	1	LED Chip select	MAX5318 DAC Chip select	2	12
13	3	MAX5318 DAC Busy	Ground	4	14
15	5	RTC Chip select	RELAY Control	6	16
17	7	3.3 V Digital	ADC Chip select	8	18
19	9	MOSI	Ground	10 20	
21	11	MISO	ADC Ready	12	22
23	13	SCLK	Not connected	14	24
25	15	Ground	Not connected	16	26

Table C.6.: JP3 pin connector enables connecting an oscilloscope to digital interface for debugging.

Pin	Function
1	LED chip select
2	MAX5318 DAC chip select
3	MAX5318 DAC Busy
4	RTC chip select
5	ADC chip select
6	MOSI
7	MISO
8	SCKL

Table C.7.: JP4 pin connector outputs control signal for the LED drivers

Pin	Function
1	Blue LED
2	Green LED
3	Red LED

Table C.8.: SV1 pin connector provides connection for a DS3432 RTC breakout board

Pin	Function
1	Ground
2	3.3 V Digital
3	Square wave (unused)
4	SCLK
5	MISO
6	MOSI
7	RTC Chip select

Table C.9.: Function of AD7175-2 ADC inputs

Input	Function
AIN0	MAX5318 DAC ground sensing
AIN1	MAX5318 DAC side of shunt resistor
AIN2	Battery side of shunt resistor
AIN3	Positive terminal of the battery (cathode)
AIN4	Negative terminal of the battery

Table C.10.: Function of AD5684R output channels

Output channel	Function
0 (A)	Red LED control signal
1 (B)	Green LED control signal
2 (C)	Blue LED control signal
3 (D)	unused

Appendix D.

Content of the DVD

The attached DVD contains:

- The screen version of this thesis.
- Eagle files with the design of the PCB
- Netbeans projects with source code of the battery testing library and applications used in testing.
- Doxygen documentation for the library.
- Raspberry Pi image
- Log files with measurements and Matlab scripts used to evaluate them.

Declaration of Self-Reliant Accomplishment of the Thesis

I declare within the meaning of section 25(4) of the Examination and Study Regulations of the International Degree Course Information Engineering that: this Bachelor report has been completed by myself independently without outside help and only the defined sources and study aids were used. Sections that reflect the thoughts or works of others are made known through the declaration of sources.

Hamburg, 9th August 2017
City, Date

Signature